A timing discriminator for space flight applications

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A timing discriminator design for space flight delay line image systems is presented. This discriminator processes delay line signal pulses having a few ns width and recovers event timing centroids with an accuracy better than 100 ps full width at half maximum. For space flight use, it is important to minimize parts count and power consumption. Because it is difficult or impossible to adjust equipment on orbit, it is very desirable to eliminate all adjustments, yet provide generous timing margins against component aging or drift. The discriminator described here uses a simple linear passive network to produce the required internal waveforms. Performance data are reported for the first flight implementation of this design. © *1998 American Institute of Physics.* [S0034-6748(98)03608-9]

I. INTRODUCTION

Delay-line readout methods for photon counting image systems[1–3] are increasingly used in space physics and astronomy missions (ORFEUS, SOHO, Lyman/FUSE, IMAGE). Delay-line readouts are attractive due to their simplicity, reliablity, and performance.

A delay-line image sensor comprises a microchannel plate, a two-dimensional delay line anode, four pulse amplifiers, four timing discriminators, and two time-interval measuring circuits. In operation, a detected event deposits charge onto the anode. The charge divides into equal portions travelling opposite directions within the anode. The output pulses have a timing relationship that is linearly controlled by the event centroid position. Each anode output feeds a pulse amplifier whose bandwidth (a few hundred MHz) controls the system noise performance and pulse shape. A fixed delay is built into one member of the *X* pair and one member of the *Y* pair to create a Start-Stop asymmetry assuring that Stop always follows Start. A timing discriminator is connected to each of these start and stop signals. The logic outputs of these discriminators drive time interval digitizers that recover each event's coordinates in real time.

Timing discriminators for these image systems are derived from existing constant fraction discriminator (CFD) designs. CFDs have been developed by many workers; see for example, the review by Spieler,[4] also.[5–8] Often however these approaches lead to flight hardware that is more complex than necessary or that fails to perform properly for pulses shorter than the propagation delays within the associated logic. In this article, I present a CFD of the arm-and-fire type whose internal zero-crossing waveform is derived from a tapped passive delay line. The design explicitly provides a large tolerance for the range of propagation delays of its control logic. The approach achieves timing performance that satisfies most delay line image system readout requirements, while offering generous margins against drift of component parameters.

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II. SYSTEM OVERVIEW

Figure 1 shows a schematic diagram for the discriminator. Comparator K1 and flip flop FF1 form a leading-edge amplitude discriminator whose purpose is to enable the timing chain, which comprises comparator K2 and flip flop FF2. This combination constitutes an arm-and-fire discriminator. The fastest commonly available logic family is emitter coupled logic (ECL), in which comparators and flip flops have propagation delays of about 2 ns, comparable to the durations of typical signal pulses being processed—a situation in which the discriminator logic planning must provide margins against timing uncertainty due to the signal pulses and due to the logic delay variations.

The innovation reported here is the use of the tapped delay line to produce a comparison waveform. Because the time duration of this waveform can be extended as far as necessary, the setup requirements for the timing comparator can be met with generous margins.

Figure 2 shows the associated timing diagram for this circuit. The upper portion of the figure illustrates the analog waveforms A, B, C, and the dc threshold level D, corresponding to the points identified in Fig. 1. The lower portion of the figure shows the status of six logic variables: D-A is the sign of K1's input, K1 is the output of comparator K1, ENA is the output of FF1, B-C is the sign of K2's input, K2 is the output of comparator K2, and OUT is FF2's output.

An incoming event that exceeds the threshold setting begins the measurement process by setting the enable state to true. Because this is a leading-edge detection, however, ENA's timing is highly variable when measured with respect to the centroid of A: as is well known the timing depends on the relationship between the input pulse amplitude and the dc discriminator setting and on the variation in propagation delay of comparator K1 with respect to varying overdrive. In practice, using 3 ns full width at half maximum (FWHM) pulses and commercially available ECL comparators, comparator K1's output, and hence ENA will vary over a range of several nanoseconds as shown in the illustration.

The timing channel of the discriminator must accommo-

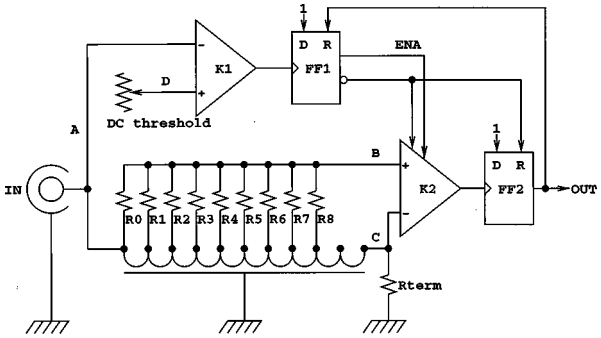

FIG. 1. Schematic diagram of the timing discriminator. Upper portion (K1 and FF1): leading-edge threshold circuit. Lower portion (K2 and FF2): timing circuit. Its novel feature is the use of a tapped delay line to create a comparison waveform at point B against which the delayed input signal C is timed.

date this varying enable timing. The tapped delay line receives the input pulse A, and creates two waveforms for the comparator: waveform B that is an unequally weighted sum of the voltages at its taps, and waveform C that is the pulse at its final output tap. The output timing is defined by the instant at which the B and C waveforms cross, identified as Tcross in the figure. The digital output is derived from this crossover by the propagation delay of K2 and the propagation delay of the flip flop FF2.

After each event, FF1 and FF2 reset themselves, and K2 is disabled to keep it from oscillating as its drive returns to zero. In counting systems where the timing output must be held TRUE until acknowledged, FF1's reset can be driven by the downstream electronics reset event rather than by FF2.

III. COMPARATOR SETUP

There are two time critical conditions imposed by comparator K2 if an arm-and-fire design is to function properly. First, the K2 input must be in its definite pre-Tcross state for at least 1 ns prior to the earliest enable. Second, Tcross must not occur until at least 1 ns after the latest enable. Together, these conditions demand that the B-C waveform be at its pre-Tcross polarity for a minimum of 5 ns. A robust design will provide generous margins beyond this minimum. In Fig. 2, B-C has its pre-Tcross polarity for about 10 ns.

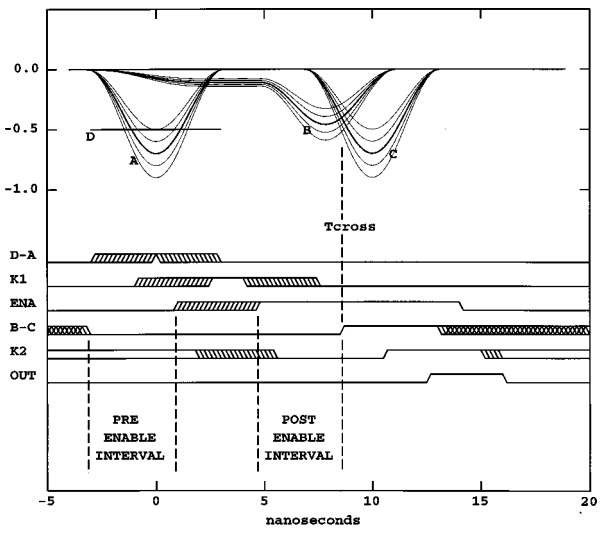

FIG. 2. Timing diagram of the discriminator. Upper portion: voltages at points A, B, C, and the dc threshold voltage D. Lower portion: logic states for six quantities described in the text—the sign of the voltage difference D-A, the output of comparator K1, the ENA state, the sign of the voltage difference B-C, the output of comparator K2, and the output logic state.

If the first condition is not met, K2's output will be undefined when enable comes true. Moreover, the necessary high gain bandwidth product of the comparator can cause instability or oscillation[9] if the comparator is enabled while its input voltage difference is zero.

If the second condition is not met, the comparator input stage will not have become fully active by the time that the zero crossing is to be detected, and large timing errors will be incurred.

The two timing conditions are sketched in Fig. 2, which shows the pre-enable interval and the postenable interval surrounding the time interval in which enable can occur. The pre-enable interval begins when the comparator input stage first sees its prebias and ends at the earliest possible enable. The postenable interval begins at the latest possible enable and ends at Tcross.

The pre-enable and postenable comparator requirements do not correspond to any of the specifications found on comparator data sheets. Those data are simple propagation delays, or describe constraints on the analog input when it is to be captured at the point where enable goes False. Experiments on AD96687 dual comparators show that allowing 1–2 ns for the pre-enable and postenable intervals gives satisfactory performance. To allow for aging and parameter drift, the present design provides for 3 ns at each interval.

In this design, the tapped delay line provides the advance warning needed to prebias the K2 input with a linear signal of the correct pre-Tcross polarity. The delay line is chosen to provide the needed comparison waveform duration. The amplitude of the comparison waveform B has to exceed the system noise and the spurious early delay line output at point C. This is easy to achieve if the front porch amplitude of B is at least a few percent of the peak amplitude of the input pulse.

The taps on the delay line are spaced by 1 ns. The resistors R0...R7 set the weights of the waveforms appearing on the taps. These resistors are 1000 ohms each. Resistor R8 at the 8 ns tap has a substantially greater weight, 100 ohms. This arrangement gives the extended front porch to waveform B, with each tap having a weight of 5%, while the single 8 ns tap has a weight of 60%. In this way the crossover between waveforms B and C occurs at about the 50% point of C, which is the theoretically optimum point for symmetric pulse shapes and in practice has proven nearly optimum for delay-line-anode image systems. Yet, as early as $t=0$, 5% of the input pulse amplitude appears at the comparator input as prebias.

The comparison waveform B is relatively free of tap ripple because the tapped delay line is composed of lumped-circuit (LC) stages that inherently act as low pass filters. The risetimes of the individual tap voltages are therefore somewhat slower than the intertap delay time, giving a smoothing behavior.

The K2 comparator enable interval ends one propagation delay after the output timing edge. At this instant, the K2 comparator input is not well determined; it depends on the irregularities and reflections that follow the main lobe of the pulse. In delay-line image systems these reflections can range up to 50% of the amplitude of the main lobe and can be of either polarity. For this reason it is not practical to force the K2 comparator into a known postevent state by extending the B or C waveforms with a back porch. The present design permits K2 to idle in either its 1 or 0 state while awaiting the next event, as shown in Fig. 2, and provides enough time for K2 to safely transition to its 0 state prior to each timing event.

IV. TEST DATA

As a prototype for the forthcoming IMAGE-FUV Spectroscopic Imager experiment, a circuit board was built comprising four CFDs, two time-to-amplitude converters (TACs), two charge to amplitude converters (QACs), four analog to digital converters (ADCs), digital data handling logic, and dc power conditioning. Comprehensive test data on the circuit, including thermal and electrical performance, were gathered. The data reported here were abstracted from those records.

The timing discriminators were implemented using Analog Devices AD96687 dual comparators[10,11] whose design derives from the Am685 described by Giles and Seales.[9] The flip flops are Motorola MC10H131 dual ECLs. The tapped delay line was a model 5P10 delay line from ESC Electronics Corporation with a 50 ohm characteristic impedance and a 10 ns end-to-end delay. In this implementation, each discriminator occupies a 7 cm×3 cm board area and consumes 0.7 W. The circuit's only adjustment is its dc threshold level, settable by telecommand.

A series of tests using bench pulsers (Hewlett Packard HP8012B and Stanford Research DG535) and a switchable delay cable (Phillips Scientific 792) were performed. Tests included temperature stability, rate sensitivity, dependence on supply voltages, dependence on pulse shape, and time resolution. An example of a resolution test is shown in Fig. 3, which is a histogram of Start-Stop timings for fixed cable-delay intervals of 8.0 and 8.5 ns. For this resolution test the input pulse amplitude was held constant. The bin size was 7.5 ps for these runs. The observed jitter is the combined timing error of the Start and Stop discriminators and the time interval digitizer. The observed FWHM of these peaks is about 23 ps (10 ps rms).

In delay-line imagers, the start pulse, and its corresponding stop pulse have equal amplitudes because they are from opposite ends of the same anode delay line driven by a single microchannel event. Individual detector pulses will have various amplitudes, but for each event start and stop are equal. Therefore the key performance characteristic of the discriminator is differential walk: the systematic variation in measured Start-Stop time difference with respect to the common amplitude of the start and stop pulse. Figure 4 shows this variation for the test article, and indicates that the extreme differential walk is about 100 ps over a 100:1 dynamic range. For these tests, the discriminators were not dewalked,

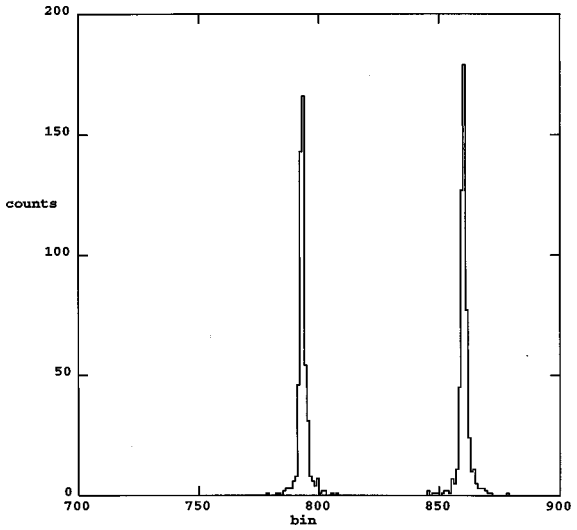

FIG. 3. Distribution of observed start-stop time intervals with stop delayed from start using a switchable delay cable. Widths of the distribution peaks measure the combined jitter of the two timing discriminators and the time-to-amplitude converter. Left peak: 8.0 ns delay. Right peak: 8.5 ns delay. For this figure the bin size is 7.5 ps and drive level is 500 mV. Observed width is about three bins or 23 ps FWHM, or 10 ps rms.

nor was any adjustment or selection of circuit components made.

Tests employing a full image system have also been run. For these, an engineering prototype detector with a two dimensional crossed delay line anode was employed, along with the associated dc high voltage supply and four-channel wideband amplifier. Briefly, the image system requirements specify a format of 1024×1024 pixels spanning a 20×20 mm field of view, a full scale timing range of 25 ns, a least significant bit resolution of 25 ps, and an overall end-to-end rms timing error of 66 ps rms. The total image blur budget has several contributions including the illuminating optics, amplifier noise, and the timing system. Single-photon microchannel plate (MCP) detectors of the type used here have a typical spread in pulse height of about 60% FWHM, which contributes to the system spatial resolution due to discriminator walk. For these image tests, events spanning a 6:1 charge range were accepted.

Figure 5 shows an image produced by illuminating the microchannel sensor through a 40×40 grid of 10 μm pin-

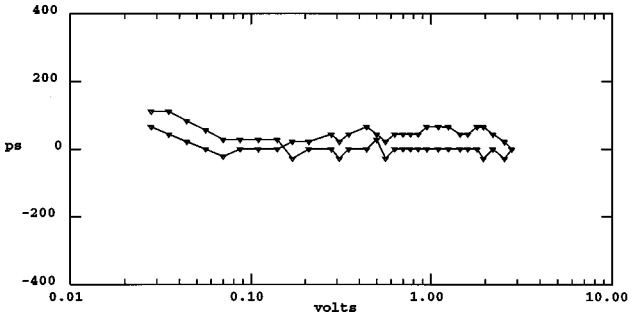

FIG. 4. Differential walk diagram showing dependence of observed start-stop time interval on input pulse amplitude. Setup is similar to Fig. 3, but the amplitudes of the start and stop pulses are varied together over the amplitude range shown. The two differential walk plots are the *X* and *Y* axes of the prototype image system.

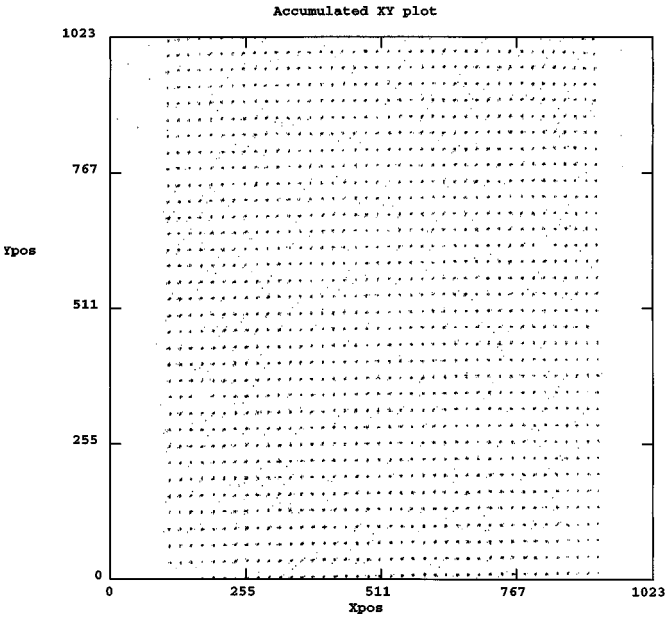

FIG. 5. Image produced by illuminating the microchannel detector with ultraviolet light through a grid of 40×40 pinholes on 0.5 mm centers. Event *X* and *Y* positions are obtained from the *X* and *Y* axis time intervals. Time range is 25 ns; bin size is 25 ps.

holes on 0.5 mm centers. The illumination was ultraviolet light from a gas discharge lamp. The histogram plotted in Fig. 6 shows the one dimensional distribution of photoevents from a small area near the center of the image. The individual intensity peaks have widths of about 3 bins which is 75 ps FWHM (30 ps rms) or, in terms of spatial resolution, 60 μm FWHM (25 μm rms). This level of performance meets our present requirements.

V. ALTERNATIVE IMPLEMENTATIONS

The tapped delay line technique for creating the reference waveform ''B'' can be tailored for a variety of applications by adopting other weighting functions and/or time scales. To obtain crossover fractions other than the 50% point used here, the weight of the final B-pulse tap can be set to whatever is needed.

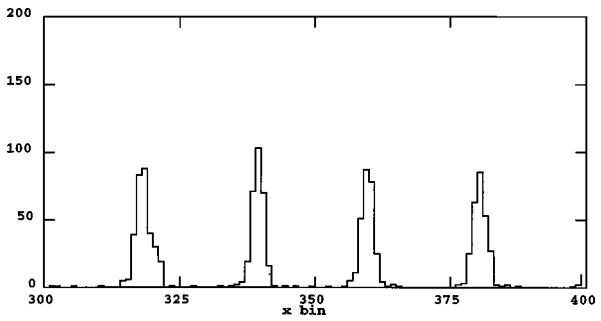

FIG. 6. Observed distribution of photoevents from the central portion of Fig. 5. Bin size is 25 ps. FWHM of the photoevent peaks is about 3 bins or 75 ps or 60 μm.

For applications in which the timing comparator must be left in a definite state after each event as recommended by Ghioni *et al.*,[8] waveform B can be extended to times later than the disable event by extending the tapped delay line to provide a back porch. To achieve a clean reset in this manner requires that the input pulse be free of overshoot and reflections immediately following the main lobe. We have not used this method here since delay-line imagers have position-dependent reverberant disturbances that follow the main pulse.

For high-speed photomultipliers that offer a subnanosecond signal waveform, the C pulse can be obtained from a separate wideband delay cable rather than from a tap on the B-pulse lumped-constant delay line. In this way the bandwidth and speed for the C pulse can be retained and the timing jitter correspondingly reduced, with no increase in active circuitry or power consumption.

For counting systems that produce a bipolar pulse rather than the unipolar pulse considered above, the zero crossing of the bipolar waveform can yield the timing crossover without need to generate a separate pulse C. To obtain the needed front porch prebias, the resistors R0...R7 should form a sequence of monotonically increasing weights. The timing event is the zero crossing of waveform B following the front porch.

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