Stacked orthogonal serpentine delay lines with vias for two-dimensional microchannel plate readout

M. Lampton[a] and M. Marckwordt
Space Sciences Laboratory, University of California, Berkeley, California 94720

(Received 24 May 2000; accepted for publication 27 September 2000)

We demonstrate a multilayer circuit board that has two orthogonal serpentine delay lines on different layers to read out event positions from a microchannel plate (MCP). The top serpentine is directly bombarded by the MCP. The orthogonal buried serpentine receives its charge through thousands of vias that connect to the top surface. Event *X* and *Y* positions are decoded with a timing circuit for each axis. The spatial resolution is much finer than the via spacing because every event's charge footprint spans several vias, and because the timing circuit senses the centroid of the event's position on each delay line. This construction method eliminates fabrication problems encountered in previous multilayer designs and eliminates the need for crossed conducting fingers with their concomitant degradation of the otherwise excellent phase delay characteristic of serpentine delay lines. Performance data are presented for an anode of this new type. Formulas and graphs are given to assist in creating a variety of anodes of this type. © *2000 American Institute of Physics.* [S0034-6748(01)00501-9]

I. INTRODUCTION

Microchannel plates (MCPs) are the basis of many position sensitive detectors. They are light in weight and have low power consumption, and yield sufficiently high gain to detect individual ions, atoms, and photons. An attractive readout method is the planar delay line, which encodes each event's position as a time difference between the pulses emerging from its two ends (Lampton, Siegmund, and Raffanti[1]). For one-dimensional (1D) readout, a planar delay line is an excellent solution. However, most sensors need at least some sensitivity to the orthogonal coordinate. The extension of the delay line concept to two dimensions has not been straightforward.

The ORFEUS spectroscopy missions used a 1D serpentine delay line for the high resolution wavelength axis, and for the second axis used a pair of coplanar wedge-wedge combs connected to an amplitude ratio circuit.[1] A variant of this idea (Lampton, Siegmund, and Raffanti[2]) used two parallel 1D delay lines sharing each event's charge. Again, timing gives the high resolution coordinate, and charge division between the two lines gives the orthogonal axis.

For fully two-dimensional (2D) work it would be very useful to use a pair of orthogonal delay lines to read out each event. One approach pursued by Siegmund *et al.*[3] uses two coplanar serpentine delay lines located just outside the working image area. Within the image area there is an array of horizontal conducting strips overlaid by an array of vertical conducting strips. The strips connect to taps on the delay lines. The strip planes are separated by insulators and an intermediate group of grounded shielding strips. This method has been used on a number of flight missions including SOHO, FUSE, IMAGE, and GALEX. There are unfortunately drawbacks to this approach. Fabrication is difficult and has a poor yield due to the need for precise alignment of the slotted dielectric layers that separate the strips vertically, and the different heights that the conducting fingers must bridge. Also, the anode has to be considerably larger than the working image area, to accommodate the outboard serpentines. Performance can suffer in larger detector formats because the finger capacitance limits the degree to which the delay lines can deliver a linear phase characteristic essential to avoid pulse dispersion, pre-shoot, and ringing.

An alternative approach due to Friedman *et al.*[4] eliminates the fingers by superposing the orthogonal serpentines on different layers within a common working image area. To allow electron access to the lower serpentine, they cut long slots into the intervening dielectric using ablative laser machining. The copper layers themselves are slotted using standard photolithography, prior to bonding the multilayer stack. This approach avoids the problems introduced by the nonlinear phase caused by fingers and eliminates the outrigger delay lines.

However, Friedman *et al.* do not address our further concerns: it is desirable to have all pickup electrodes coplanar, to eliminate the efficiency dependence on the exit angle distribution of electrons emerging from a biased MCP. Having all electrodes coplanar also simplifies positionally registering them in two dimensions because they would then all be formed in a single photolithographic step. Further, it is desirable to eliminate the costly laser ablative slotting process in favor of a simple repetitive mechanical or laser drilling process such is used in conventional circuit board fabrication. Unlike slotting, drilling retains nearly all the strength, dimensional stability, and stiffness of the parent laminate. With drilling, anodes could be fabricated as easily as other circuit boards, thereby reducing cost and manufacturing lead

[a]Electronic mail: mlampton@SSL.berkeley.edu

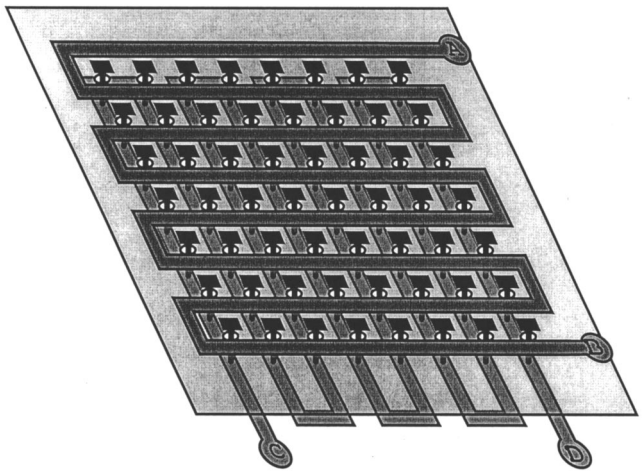

FIG. 1. Plan of the orthogonal-serpentine anode using vias. The top serpentine delay line receives charge from the MCP above the anode. A ground plane (shaded) serves to terminate the field lines from the serpentine, so that it behaves like a microstrip transmission line. An orthogonal serpentine on the bottom provides the second sensor dimension. It receives charge from the top through several thousand vias that pass through the ground plane but do not connect to it.

time, yet would offer excellent stiffness, strength, and dimensional stability.

One obvious way to conduct electricity from the front of a circuit board to a buried layer is to use conductive vias. These are drilled holes that are plated through with copper. Vias are found by the thousands in PCs and other electronics. In commercial production, vias are cheap and reliable. In this article we report our first experimental anode that uses vias to conduct a portion of each event's charge to a buried serpentine.

II. ANODE CONCEPT

The design adopted here derives from a simple one-dimensional delay line anode often used in laboratory demonstrations. This single serpentine readout system has two copper layers separated by an insulating layer. The top copper layer is the serpentine pattern, and the bottom layer is a continuous ground plane. The combination is a folded-up microstrip transmission line whose characteristic impedance and propagation speed are chosen using standard engineering design formulas (see the Appendix).

Our 2D design is shown schematically in Fig. 1. The top copper layer is again a serpentine, and the second copper layer is a ground plane. To achieve 2D sensing, there is a third copper layer having an orthogonal serpentine pattern. To bring incoming charge to the third layer, the circuit board has several thousand conductive vias that penetrate the dielectric layers and the ground plane. At the top of each via is a small copper pad, coplanar with the top serpentine, that receives charge from the MCP. The aggregate area of the pads is chosen to collect about half the incident charge and deliver it to the buried serpentine where it is used to obtain the second readout axis. The other half of the charge is received by the top serpentine in the usual way.

There is an optional fourth copper layer not shown in Fig. 1: Another ground plane, identical to the second layer

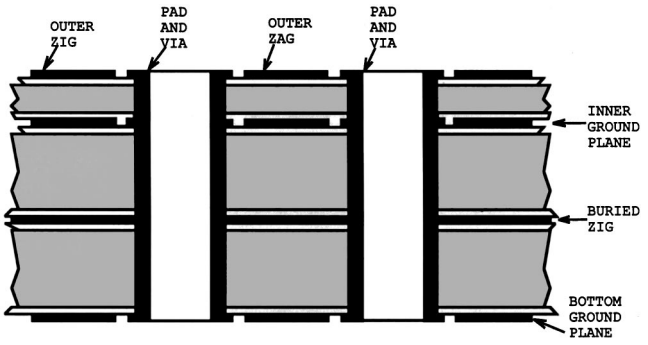

FIG. 2. Cross sectional diagram of the orthogonal serpentine anode showing four copper layers. The dielectric surrounding the buried serpentine is thicker than the dielectric supporting the top serpentine so that the impedances come out about equal.

ground plane, that shields the bottom of the second serpentine. Figure 2 shows a cross sectional drawing with this configuration.

There is a distinction to be drawn between the exposed top serpentine and a buried fully shielded serpentine. When buried between two conducting ground planes, a conductor is described as a stripline, and its propagation is accurately described by a transverse electromagnetic (TEM) mode in a homogeneous dielectric medium. The top serpentine, however, sees vacuum on one side and the dielectric substrate on the other side. This inhomogeneous environment is described by the slightly more complicated quasi-TEM microstrip equations. We have summarized the properties of these delay lines in the Appendix.

III. MATERIALS

Due to its excellent electrical conductivity, solderability, and adhesion, copper is almost always used as the conductor material in circuit boards. However, there is a wide choice of dielectric materials. In Table I we list some alternatives from the many that are commercially offered, gleaned from microwave handbooks and manufacturer data sheets. In this table, K lists the value of the dielectric constant relative to vacuum and D is the dimensionless dissipation constant $\tan(\delta)$. The maximum service temperatures of the polymer based materials ranges from 120 to about 260 °C, while the ceramics glasses and crystals can go much higher, into the temperature range appropriate for UHV bakeout.

TABLE I. Dielectric materials.

Material	MFR.	K	D
NEMA FR-4 fiberglass epoxy	GE;others	4.0	0.02 up
Fiberglass PTFE	Many	2.2	0.001
AR-85N fiberglass polyimide	Arlon	4.2	0.013
AR-1000 PTFE alumina	Arlon	9.0	0.0002
TMM family PTFE ceramic	Rogers	Several	0.0001
RO-3000 PTFE ceramic	Rogers	Several	0.0013
Alumina, purity 0.996	Coors	9.3	0.0001
Beryllia, purity 0.995	Brush	6.9	0.0002
Borosilicate glass	Corning	4.3	0.0003
7059 glass	Corning	5.8	0.0001
Fused silica	Heraeus	3.8	0.0001

For our initial efforts described here we adopted Arlon 85N material, which is a fiberglass and polyimide composite. It is available in a range of thicknesses and can be laminated using commonly available bond films. Its advantages include good bonding [no polytetrafluoroethylene (PTFE)], reasonable dielectric constant and tolerable dielectric loss. In woven laminate form its vertical coefficient of thermal expansion is matched to that of copper, to avoid stressing vias under thermal cycling. It is considered easy to mechanically drill compared to composites that contain alumina or other hard minerals. It is, however, not bakable beyond about 120 °C. For our demountable test detector work we do not perform bakeouts and are therefore not concerned with its service temperature limit.

IV. DESIGN DETAILS

To begin the design process we adopted a working field area of 50 by 50 mm. For convenient connections to lab pulsers, scopes, amplifiers and cables, we sought a characteristic impedance close to 50 Ω for both the top serpentine and the buried serpentine. For fabrication feasibility we chose a conductor width $W=0.3$ mm (12 mils) for each serpentine, and a minimum gap width between neighboring conductor edges equal to 0.125 mm (5 mils). This combination gives a full period (zig + vias + zag + vias) equal to 1.7 mm (68 mils) and a serpentine filling factor of 0.35. There are 30 zigzags in each serpentine, and the number of vias is $60\times59=3540$. The conductor width is compatible with a 0.25 mm (10 mil or number 80) carbide drill commonly used for plated-through hole vias. The unfolded length of the serpentine is 3.0 m, and the serpentine folding factor (the ratio of the folded length to the unfolded length) is 0.017. The ratio of unfolded length to conductor width for this pattern is 10 000, and the end-to-end dc resistance of each serpentine should theoretically be 5.5 Ω with our nominal 33-μm-thick (1 oz) copper.

A. Top delay line

Our adopted dielectric material has $K=4.2$, which requires a ratio $W/H=2.0$ to give a 50 Ω impedance according to the microstrip design information in the Appendix. This fixes $H=0.15$ mm (6 mils) which is conveniently obtained with a standard sheet thickness of 5 mils plus the requisite two bond films. The microstrip propagation speed will be 0.59c. The net speed along the encoding axis for the top serpentine is the product of this straight line speed and the folding factor, 0.010c or 3 mm/ns. Its nominal one way delay $T=17$ ns for the 50 mm field of view. The actual delay turned out to be somewhat greater than this estimate owing to the added paths and delays introduced at the hairpin turns.

B. Buried delay line

We chose to make the buried serpentine have a nominal impedance of about 50 Ω also. From Fig. 11 this requires $W/H=1$ and for our choice of W this requires that the dielectric be about twice as thick as for our microstrip, namely 0.25 mm (10 mils). With the additional bond film, this choice gives $H=0.28$ mm (11 mil) and speed 0.50c. The net speed along the encoding axis is then 0.0085c and the nominal one way delay is $T=19.6$ ns for the 50 mm field of view. This delay turned out to be considerably greater as a result of its hairpin bends and the added capacitive loading introduced by the 3540 vias distributed along its length.

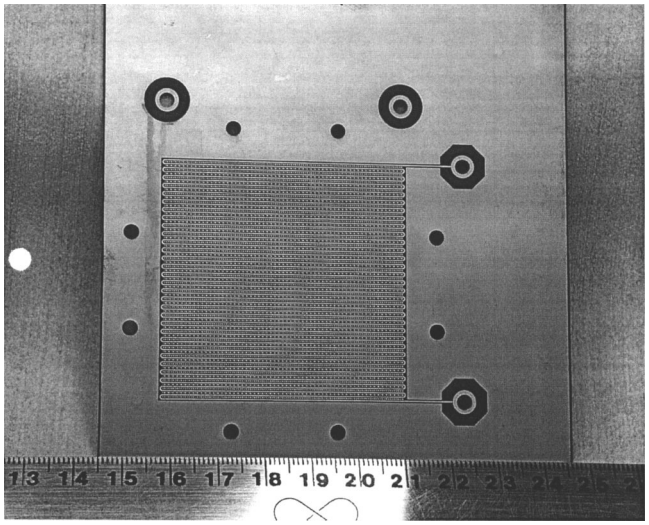

FIG. 3. Photograph of the top face of an orthogonal serpentine anode using vias. The top pads of the vias are coplanar with the top serpentine. The anode period is 1.7 mm. The vias are spaced 0.85 mm in both *X* and *Y*.

V. FABRICATION

Fabrication was performed by a local circuit shop using conventional PCB technology. The board is built up starting from its central dielectric layer to which copper foils are bonded. After lamination, the copper is cleaned, coated with photoresist, exposed through a carefully registered layout negative, etched, and again cleaned. Then the outermost layers and foils are bonded. Then, the board is robotically drilled and the vias are plated through. Finally, the outermost copper foils are coated with resist, exposed, etched, and cleaned. The misregistration of the inner layers does not affect the dimensional accuracy of the charge collecting electrodes, which is entirely defined by the top copper layer.

A photograph of our anode is shown in Fig. 3. Here, the via pads are visible as rectangular patches lying between the zigs and zags of the top layer serpentine. Charge landing on the insulator is not lost: It immediately builds a negative potential that guides subsequent electrons to the neighboring conductors.

VI. BENCH TESTING

Bench testing began with ohmmeter checks for shorts and opens. In our first batch of six anodes, only one short was found. The dc resistance of the top and buried delay lines measured 8 and 9 Ω, respectively. The capacitance of the top delay line to ground was 400 pF measured at 1 kHz, in tolerable agreement with the 330 pF prediction from microstrip theory. The buried delay line was 810 pF, significantly greater than the 440 pF expected. This excess may be

an indication of the extra capacitive loading due to the vias; if so, each via contributes about 0.1 pF to its serpentine's capacitance.

Pulse testing of the anode in air was performed by driving each of the four anode terminals with a Stanford Research DG-535 pulse generator and observing the waveforms at the other terminals with a Tektronix TDS-620B oscilloscope. If the delay lines were free from preshoot, ringing, overshoot, and other manifestations of a nonlinear phase characteristic, each output wave form ought to be quiet until the full propagation time has elapsed, at which point the pulse ought to appear with nearly its full amplitude and very little broadening in time. If the delay lines were free from cross talk, a pulse on the *X* axis ought to couple no signal into the *Y* outputs, and vice versa.

Figure 4 shows the overall timing picture. The top trace is the input pulse from the generator, 1.5 V in amplitude and 4 ns full width at half maximum (FWHM), loaded by a 50 Ω terminator. (There is a small reflection afterpulse visible.) The middle trace shows the output from the top delay line; the wave form is quiet until the pulse emerges at 20 ns. The end-to-end attenuation is seen to be about 3 dB, in tolerable agreement with the simple formula in the Appendix that predicts 2.3 dB at 100 MHz. The bottom trace shows the output from the buried delay line; again, it is quiet until the output emerges at 28 ns. The narrowness and symmetry of the output pulses speak for their freedom from phase distortion and dispersion.

Figure 5 documents the freedom from early spurious disturbances. Like Fig. 4, the top trace is the input pulse. The outputs shown in the middle and bottom traces have been magnified to a display scale of 10 mV/div. Early disturbances are only about 0.3% for either axis.

Figure 6 shows the cross talk performance. Here, one delay line is pulsed while we observe the other under high gain. In either direction the cross talk is about 1.5% or −36 dB.

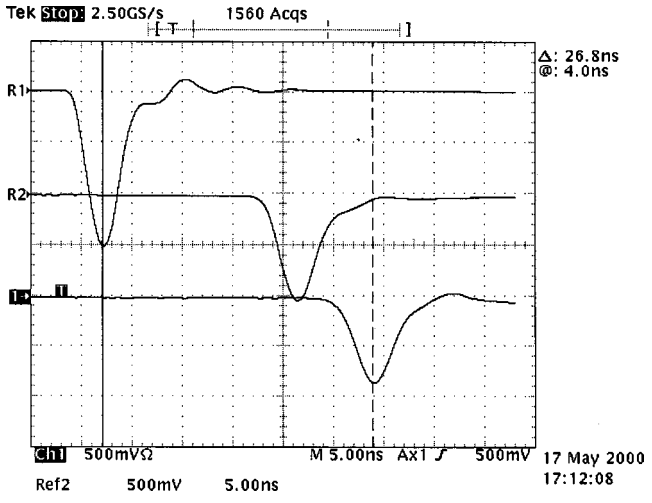

FIG. 4. Oscillogram showing the propagation of a 4 ns pulse introduced simultaneously at one end of each serpentine. Upper trace: input pulse. Middle trace: far end of top serpentine, showing one-way delay of 20 ns. Lower trace: far end of buried serpentine, showing one-way delay of 28 ns. Evidence of the excellent phase linearity is the narrow pulse width, the equal rise and fall times, and the absence of pre-shoot, overshoot, and ringing.

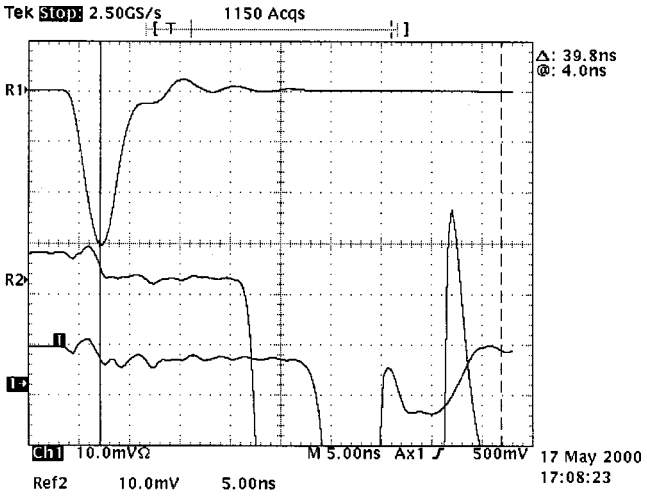

FIG. 5. Like Fig. 4 but with higher gain (10 mV/div) on the two output channels, to show the relative freedom from unwanted early disturbances appearing at the delay line outputs. On either line, the early disturbances are about 0.3%.

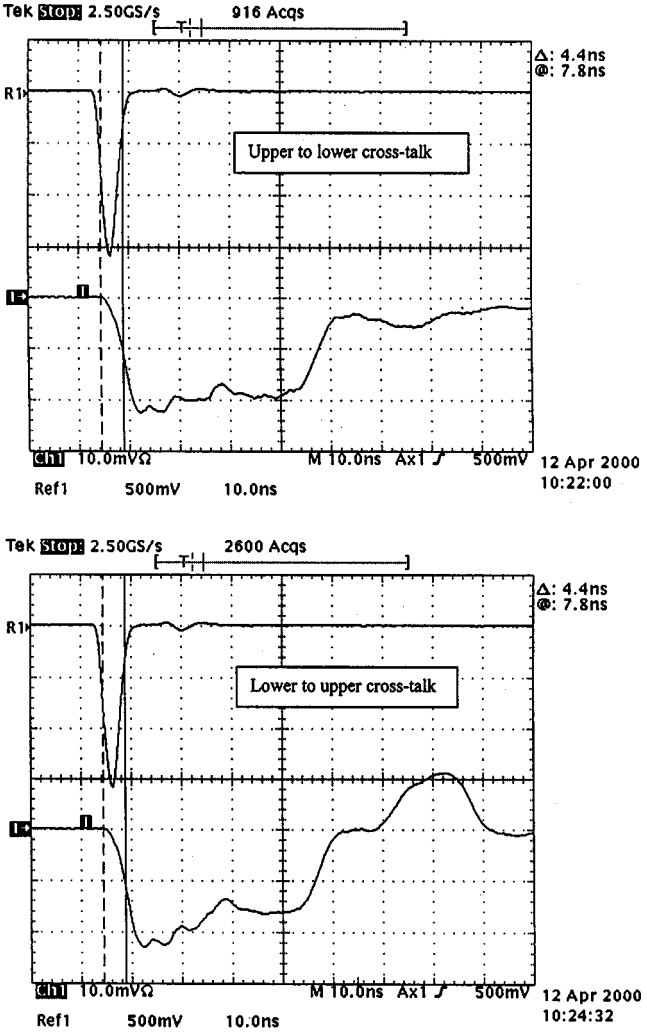

FIG. 6. Oscillograms showing cross talk. Upper portion: pulser drives top serpentine, buried serpentine output shown. Lower portion: pulser drives buried serpentine, top serpentine output shown. Either way the cross talk is about 1.5%.

VII. IMAGE TESTING

Image testing of the anode was performed by mating it to a MCP detector borrowed from another project. The detector was a *Z* stack of MCPs, each being 33 mm diameter, 80:1 length/diameter, 13° bias angle, 2600 MΩ total dc resistance in vacuum. The anode was attached to an aluminum plate that facilitated electrical connections through four coaxial signal cables and a high voltage cable. The spacing between the MCP exit face and the anode was 11 mm. Outside the vacuum chamber we connected four wideband pulse amplifiers and a two-axis time interval digitizer (Lampton[5]) borrowed from the IMAGE-FUV program. Data were gathered on a computer borrowed from the CHIPS project. Owing to the small diameter of the MCP stack and its mounting hardware, only a fraction of the anode field of view could be explored with this setup. Nonetheless, we were able to establish reasonable imaging performance as described below.

Initial pumpdown and turn on showed satisfactory MCP behavior. With a bias of −3400 V on the MCP front face and −944 V on the exit face, the background rate in the cryopumped vacuum chamber was 15 cps. With ultraviolet illumination the breadth of the MCP pulse height distribution measured 80% FWHM indicating acceptable electron gain saturation. The mean event pulse height was 1.0 pC.

For a subsequent imaging run we fastened a perforated metal mask onto the entrance face of the detector to establish a known grid of event positions. This mask had a regular grid of pinholes on 2 mm × 4 mm centers. Each pinhole was 50 μm in diameter. The mask was clamped onto the face of the MCP detector and the system was illuminated by flood UV radiation from outside the chamber through an UV transmitting porthole.

The images obtained in this way are reasonably good over the central part of the MCP working area. An example is shown in Fig. 7. Approaching the boundary of the MCP there is noticeable barrel distortion arising from the nonuniform electrostatic fields caused by our MCP rear mounting plate. Figure 8 shows a two-dimensional histogram of events occurring in part of the central uniformly mapped area. One-dimensional slices are plotted in Fig. 9 where the time resolution is 24 ps/bin. Using the grid periods as distance calibrators, we derive the linear scale factors for *X* and *Y*: 23 and 27 μm/bin, respectively. The peaks are only about two bins wide (indeed these peaks are about the same size as the pinholes in our target mask) so at present we have only a crude upper limit to the detector resolution, 50 μm.

VIII. FUTURE WORK

Many directions for future improvements are becoming apparent. For detectors that are to be baked for ultrahigh vacuum work or for sealed getter-pumped tubes it is vital to adopt high-temperature inorganic dielectric materials for the anode. Fortunately, the microwave industry has developed multilayer ceramic circuit technology, including metallized vias, that could be adapted to the present anode concept. Ceramic technology is also attractive from the standpoint of improved lithographic pattern accuracy.

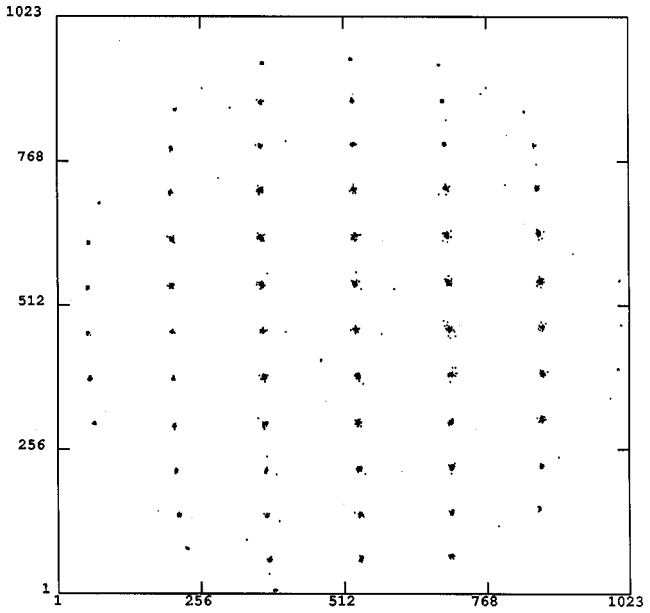

FIG. 7. An image taken with the stacked serpentine anode. A *Z* stack of three 25 mm microchannel plates was mounted 11 mm above the anode. The MCP entrance face was biased to −3400 V and the exit face was biased to −944 V with respect to ground. Photons from a Pen-Ray ultraviolet lamp flood a perforated metal mask attached to the MCP face. The perforations are 50 μm diameter on a 4 mm × 2 mm grid, from which the linear scale of the image is determined. The edge distortion is believed to be caused by the focusing effect of the rear clamping plate for the MCPs.

Meanwhile, co-workers have suggested a variety of alternative conductor and layer patterns. Carlson has proposed burying both delay lines between ground planes and feeding both from a double density grid of vias. In this way the axes would have the same delay and impedance characteristic. Another idea is to arrange polar coordinate readout for beam scattering experiments, with a spiral stripline giving the radial coordinate. Upcoming projects may permit some of these avenues to be explored.

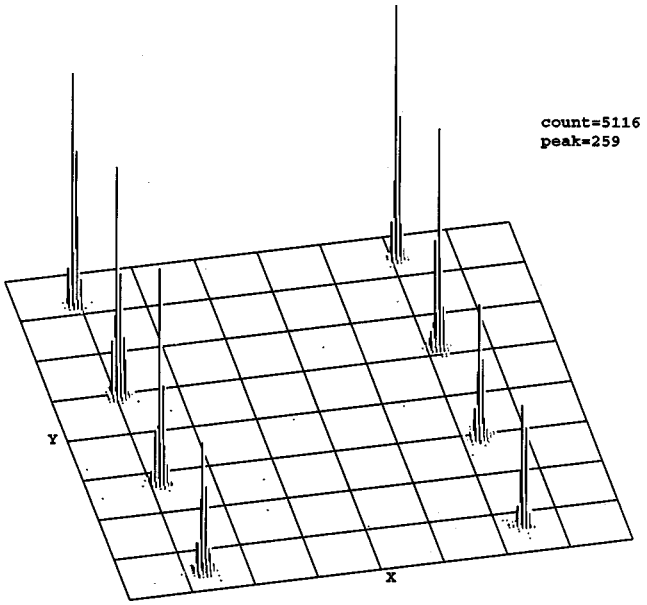

FIG. 8. Two-dimensional histogram of events from the central region of the field of view.

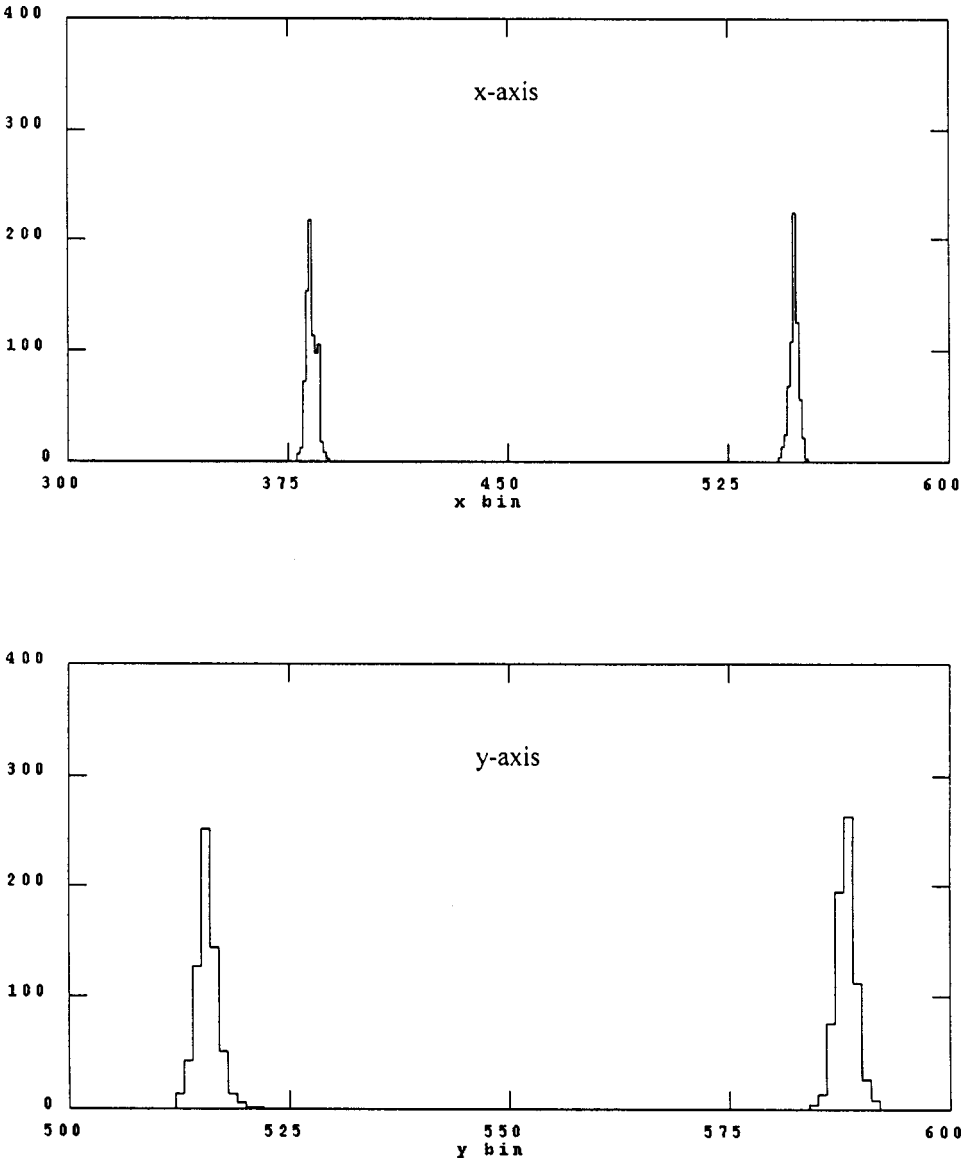

FIG. 9. Upper diagram — histogram of *X* axis coordinates of a portion of the events seen in Fig. 7. The position resolution is roughly two bins FWHM (1 bin = 24 ps). Using the scale factor derived from the spacing of the peaks and the known pinhole spacing, this is 46 μm FWHM. Lower diagram — histogram for the *Y* axis; FWHM = 2 bins or 54 μm. Because the pinholes are about the same size as these distributions we regard these widths as upper limits to the anode performance.

ACKNOWLEDGMENTS

The authors gratefully acknowledge support from Space Sciences Laboratory and the encouragement of Director R. P. Lin. The authors thank Dr. S. Mende for loaning them several pieces of hardware from his IMAGE-FUV project. They thank R. Herman for his many suggestions and assistance with the layout and R. Appledorn at BoardWorks of Oakland, CA, for his guidance during the fabrication process.

APPENDIX: DELAY LINE THEORY

1. Propagation

For a straight transmission line, the voltage $v(x)$ and the current $i(x)$ are connected through a pair of sine wave equations

$$dv/dx = -(R + j\omega L)i,$$

$$di/dx = -j\omega C v,$$

where L=inductance per unit length, C=capacitance per unit length, and R=alternating-current resistance per unit length. The time dependence of both e and i is $\exp(j\omega t)$. In terms of the voltage alone

$$d^2v/dx^2 + k^2 v = 0,$$

where $k^2 \equiv \omega^2 LC - j\omega RC$. Here we assume that k^2 is uniform, that is L, C, and R are constant with respect to position along the transmission line.

There are two wave solutions for these equations propagating in opposite directions with the form $\exp(\mp jkx)$. We now decompose k into its real part β that describes the phase characteristic and its imaginary part α that describes the attenuation

$$\beta = \omega\sqrt{(LC)} = \omega/v_{\text{phase}},$$

$$\alpha = \frac{1}{2}\beta D + \frac{1}{2}\frac{R}{Z}.$$

Here, β is expressed in radians per meter and α is expressed in nepers per meter (1 neper = 8.686 dB). For these expres-

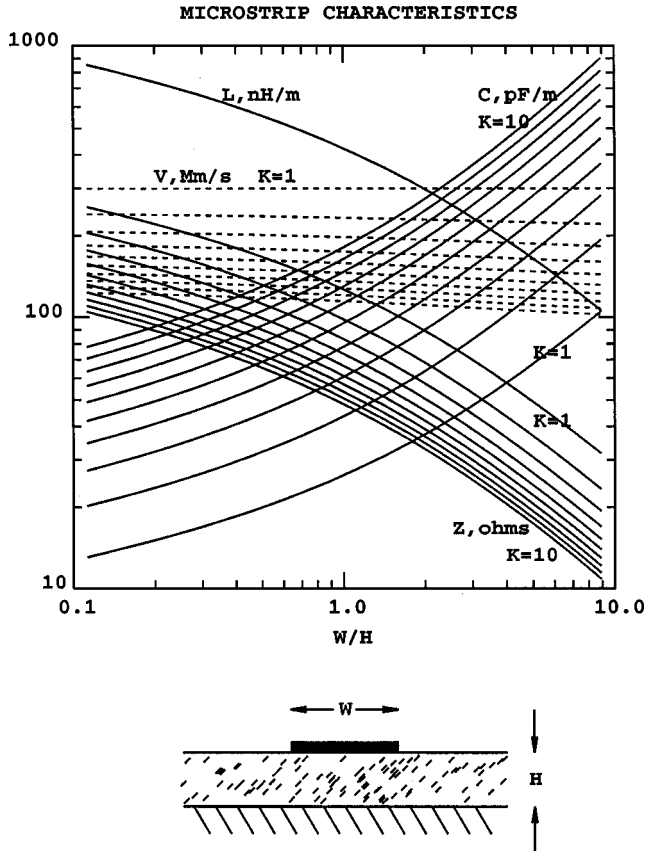

FIG. 10. Characteristics of microstrip. For values of the dielectric constant $K=1-10$, four quantities are plotted as functions of the ratio of the dimensions W and H shown. L is the inductance per unit length; C is the capacitance per unit length; Z is the characteristic impedance; V (dotted) is the propagation speed.

sions we have made two substitutions: Z represents the characteristic impedance of the delay line, $\sqrt{(L/C)}$. We have allowed for dielectric dissipation by replacing the real capacitance C by an expression having a small explicit imaginary part, $C^*(1-jD)$, where D represents the dimensionless dielectric dissipation factor.

These two loss terms have differing frequency dependences. The dissipation term increases approximately linearly with frequency because β contains the factor ω and D is nearly constant. In contrast, the resistance loss increases only as the square root of frequency owing to the skin depth. With most dielectric materials, the resistance term dominates the loss expression at frequencies of the order of 100 MHz.

2. Straight microstrip

Figure 10 shows the design curves computed from Gupta, Garg, and Chada[6] [Eq. (3.66) p. 66] for the case of a straight microstrip. Because the dielectric medium is inhomogeneous (vacuum above the conductor, substrate below) the low-frequency propagation mode is referred to as quasi-TEM rather than TEM. For given dimensions W and H, and for a given dielectric constant K relative to vacuum, the solid curves show the inductance L per unit length, the capacitance C per unit length, and the characteristic impedance Z in ohms. The dotted curves show the propagation speed in Mm/s. In this plot the conductor thickness was assumed to be thin compared to W and H.

Resistive losses in straight microstrip can be understood in terms of a geometrical model appropriate for $W \gg H$ having two uniform current slabs and no fringing. One slab is the underside of the top conductor; its width is W (the same as the conductor) and its thickness is the skin depth δ. The other slab is the corresponding equal zone on the ground plane. For a propagating wave these two resistances are in series: $R=2R_{\text{square}}/W$ where R_{square} is the surface resistivity of the conductor (0.0025 Ω/square for copper at 100 MHz).

Resistive attenuation also requires a model for the line impedance. In the limit of large W/H, $Z=(377/\sqrt{K})*(H/W)$ Ω, where 377 is the impedance of free space and K is the dielectric constant. We combine R and Z to obtain the asymptotic (large W/H) sine wave attenuation rate

$$\alpha = 5.8\times 10^{-5}\,\frac{\sqrt{f_8}\sqrt{K}}{H}\text{dB/m},$$

where f_8 is the frequency in units of 100 MHz and H is the dielectric thickness in meters. This model, for example, predicts that a copper microstrip with a $K=4$ dielectric 0.15 mm thick will have a loss of 0.77 dB/m at 100 MHz when $W \gg H$. More accurate treatments[6] are in reasonable agreement with this attenuation model for large W/H but show rising losses as W/H decreases: about 30% greater attenuation at $W/H=1$ than at large W/H.

3. Straight stripline

Figure 11 shows the design curves computed from Gupta, Garg, and Chada[6] [Eq. (3.35) p. 57] for the case of a straight stripline. The conductor is buried within a single dielectric medium and the low-frequency propagation mode is TEM. For given dimensions W and H, and for a given dielectric constant K relative to vacuum, the curves plotted show the inductance L per unit length, the capacitance C per unit length, and the characteristic impedance Z in ohms. The dotted curves show the propagation speed in Mm/s. In this plot the conductor thickness was assumed to be thin compared to W and H. Comparing this figure with Fig. 10, it will be seen that the stripline inductance is somewhat lower, the capacitance is nearly twice as great, the impedance is about 0.6 as large, and the propagation speed is about 0.8 as great.

Resistive losses in striplines can be modeled in the same manner as for microstrip. Here, four current slabs are needed: The two center conductor slabs are in parallel as are the ground slabs, so the total resistance is half as great as for microstrip. In the no-fringing limit $W \gg H$, however, the characteristic impedance is also half as great as for microstrip with the same W, H, and K. The consequence is that the attenuation coefficient is the same; it is as if the stripline is merely two back-to-back microstrips in parallel.

4. Serpentines

Serpentine delay lines have some slight capacitive and inductive coupling from each straight segment to its neighbors. Moreover, at the end of each straight segment, there is a shift in the local impedance and propagation speed owing

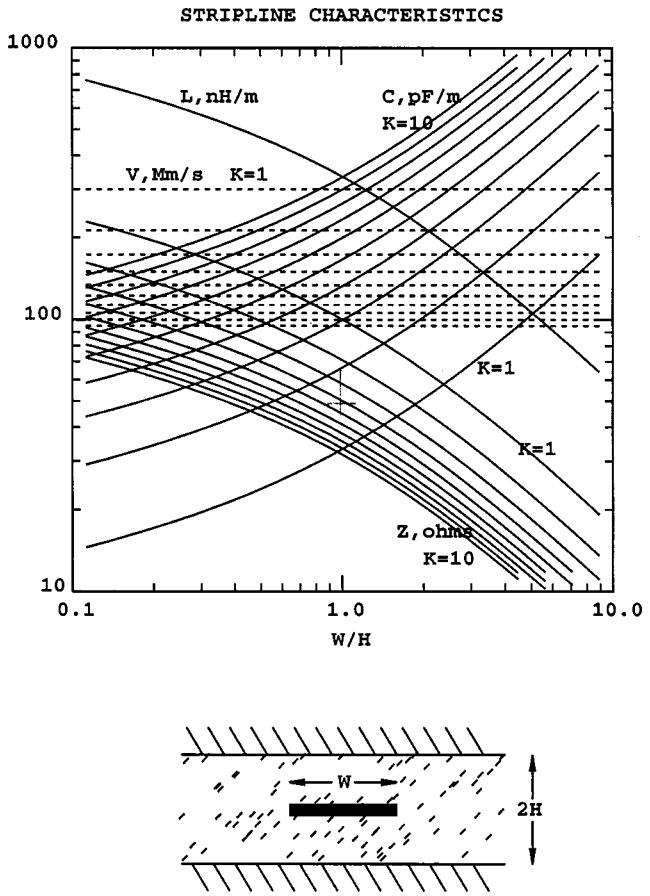

FIG. 11. Characteristics of stripline. For values of the dielectric constant $K=1-10$, four quantities are plotted as functions of the ratio of the dimensions W and H shown. L is the inductance per unit length; C is the capacitance per unit length; Z is the characteristic impedance; V (dotted) is the propagation speed.

to the 180° bend. These effects conspire to give a periodic variation in the propagation number k; that is, k can be written as $k_0+P(x)$ where P is a function that is periodic in x. The consequence is that propagation becomes dispersive, with different frequency components of a pulse acquiring different propagation speeds. The dispersion can be severe if the propagating wavelength approaches the period of the perturbing function P. We have found dispersion to be unimportant as long as the separation of neighboring conductor segments is at least as big as the dielectric thickness and the serpentine segment length is kept much shorter than the wavelengths of the principal Fourier components of the pulses being measured. In what follows we simply ignore the serpentine pattern, and regard its propagation as equivalent to the propagation in an unfolded or straightened-out line.

5. Packaging constraint on *l*/*W*

The working area is shared between the top serpentine and the via pickup electrodes. If anode image area is denoted A, the length × width product of the serpentine conductor is

$$lW=FA,$$

where the filling fraction F must be somewhat less than 0.5, limited by fabrication design rules. The serpentines described in this article have $F=0.35$.

6. Loss constraint on *l*/*W*

The end-to-end attenuation of the serpentine is given by the product $l\alpha$ which we can estimate from the simple loss model presented above

$$l\alpha=5.8\times10^{-5}\frac{l}{H}\sqrt{(f_8K).}$$

When we set this loss equal to 3 dB, f_8 becomes the 3 dB bandwidth B_8 and

$$l/H=\frac{52\,000}{\sqrt{(B_8K)}}.$$

We eliminate H in favor of W by using the asymptotic impedance model $Z=(377/\sqrt{K})*(H/W)$ to obtain

$$l/W=137Z/\sqrt{B_8}$$

which suggests that a delay line with $Z=70\ \Omega$ can have an aspect ratio of about 10 000 if its bandwidth is of the order of 100 MHz. Our serpentines have $l=3$ m and $W=0.3$ mm, which is a ratio of 10 000, and have bandwidths of the order of 100 MHz, in reasonable agreement with this picture.

7. Synthesis given bandwidth

The preceding material shows how a given format size constrains the product lW, and how a given 3 dB bandwidth fixes the aspect ratio l/W. Given both constraints, l and W are determined separately

$$l=12\sqrt{\left(\frac{FAZ}{\sqrt{B_8}}\right)},$$

$$W=0.085\sqrt{\left(\frac{FA\sqrt{B_8}}{Z}\right)}$$

from which we conclude that for a given bandwidth all dimensions scale linearly with format size, and every square 100 MHz 50 Ω delay line will be the same, having 30 zigzags in each plane and 3540 vias. On the other hand, if W, Z, F, and A are given, the 3 dB bandwidth in units of 100 MHz becomes

$$B_8=\frac{20\,000Z^2W^4}{F^2A^2}$$

from which it is clear that a narrow conductor width W imposes a severe bandwidth restriction.

8. Resolution

Factors that control the spatial resolution of delay line readouts are signal charge Q, the system bandwidth, and the system noise power spectral density U which is the product of Boltzmann's constant and the system temperature (Lampton and co-workers[1]). For best results the system bandwidth should be matched to the anode bandwidth; therefore anode design affects resolution. Ignoring gnarly constant factors of the order of unity, we adopt for the rms timing error the expression

$$t_{\mathrm{rms}}=\frac{1}{Q}\sqrt{\left(\frac{U}{B^3Z}\right)}$$

which for a typical system having an effective noise energy $kT=U=10^{-20}$ J, bandwidth $B=100$ MHz, impedance $Z=50\ \Omega$, a signal charge of magnitude $Q=10^{-12}$ C gives $t_{\mathrm{rms}}=14$ ps. Workers using other values of MCP gain can expect the time resolution to vary inversely with Q, as shown by this expression. The corresponding spatial blur, for $v_{\mathrm{strip}}=0.5c$, is proportional to this timing error

$$x_{\mathrm{rms}}=\frac{cS}{4l}t_{\mathrm{rms}},$$

where $S=\sqrt{A}$ represents the anode linear size. The corresponding number of resolution elements n_{rms} is

$$n_{\mathrm{rms}}=S/x_{\mathrm{rms}}=\frac{4l}{ct_{\mathrm{rms}}}.$$

Since we can do nothing about 4 or c, it is the l/t_{rms} ratio that controls the number of pixels available to each axis. Since $l\sim S\times B^{-1/4}$ and $t_{\mathrm{rms}}\sim B^{-3/2}$, it follows that $n_{\mathrm{rms}}\sim S\times B^{5/4}$.

[1] M. Lampton, O. H. W. Siegmund, and R. Raffanti, Rev. Sci. Instrum. **58**, 2298 (1987).
[2] M. Lampton, O. H. W. Siegmund, and R. Raffanti, IEEE Trans. Nucl. Sci. **37**, 1548 (1990).
[3] O. H. W. Siegmund, J. Stock, R. Raffanti, D. Marsh, and M. Lampton, Proceedings of the 10th International Colloquium on UV and X-ray Spectroscopy of Laboratory and Astrophysical Plasmas, Cambridge, England, 1992; O. H. W. Siegmund, M. Gummin, J. Stock, D. Marsh, R. Raffanti, and J. Hull, Proc. SPIE **2006**, 176 (1993).
[4] P. G. Friedman, R. A. Cuza, J. R. Fleischman, C. Martin, D. Schiminovich, and D. Doyle, Rev. Sci. Instrum. **67**, 596 (1996).
[5] M. Lampton, Rev. Sci. Instrum. **69**, 3062 (1998).
[6] K. C. Gupta, R. Garg, and R. Chada, *Computer Aided Design of Microwave Circuits* (Artech House, Dedham, MA, 1981).