Readout ASIC for MPGD

General Description

The ASIC constitutes the multiple anode of the **M**icro**P**attern **G**as **D**etector. Each of the 22'080 pixel elements is composed of a hexagonal electrode (top layer of metal) connected to a charge-sensitive amplifier followed by a shaping circuit. The circuit is organized in 8 identical clusters of 2760 pixels (20 rows of 138 pixels each) with an independent differential analog readout buffer. Each cluster also features customizable self-triggering capability. Upon the activation of an external digital control input, or from on-chip wired-OR combination of each cluster self-triggering circuit, the maximum of the shaped pulse is stored inside each pixel cell for subsequent readout. The latter is accomplished by sequentially connecting the output of each cell to the analog bus common to each cluster. For this purpose each pixel includes a shift register element, which can also be used to selectively stimulate the cell for electrical test and calibration.

Features

- 0.35um, 3.3V CMOS process implementation
- 80um pixel pitch (11x11mm^2 active area for 22'080 pixels)
- 4us typical shaper peaking time
- 120e$^-$ typical ENC
- 50uW per pixel typical power consumption
- global self-triggering function with adjustable threshold (set independently per cluster)
- fast serial analog readout: 100ns/pixel (< 300us total readout time for 8 x 2760 pixels)
- on-chip electrical test capability with single pixel stimulation

Absolute Maximum Ratings

Parameter	Limit value	Unit
ESD tolerance of standard I/O's (HBM: 1.5 kΩ in series with 100 pF)	1	kV
ESD tolerance of pixels pads (note 1)	100	pC
Max supply voltage (VDD– VSS)	3.6	V
Max voltage at any pin	VDD + 0.3	V
Min voltage at any pin	VSS – 0.3	V
Continuous total dissipation (T_{amb} < 60°C)	2000	mW
Derating factor above T_{amb} = 60°C	5	mW/°C
Storage temperature range	−65 to +125	°C
Junction temperature	−40 to +125	°C

Note 1: The pixel pads are not equipped with an ESD protection device other than the parasitic drain-to-bulk junctions of functional devices. Therefore extreme care has to be taken when manipulating the ASIC alone to avoid electrical damage to the circuit by electrostatic discharge through pixel pads.

Operating Ratings

Parameter	Limit value	Unit
Max supply voltage (VDD – VSS)	3.6	V
Min supply voltage (VDD – VSS)	3.0	V
Operating temperature range, T_{amb}	−40 to +85	°C

Simplified Equivalent Schematics

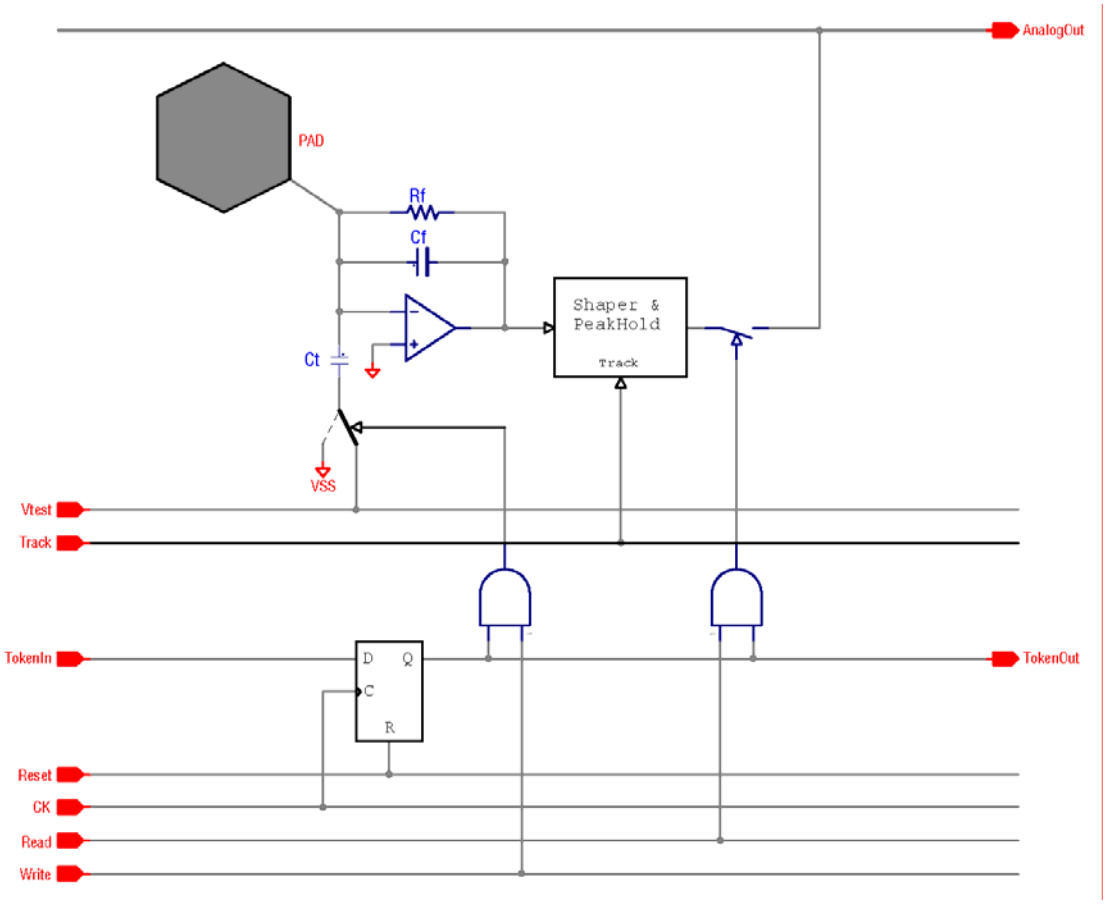

Figure 1: Simplified equivalent schematic of 1 pixel

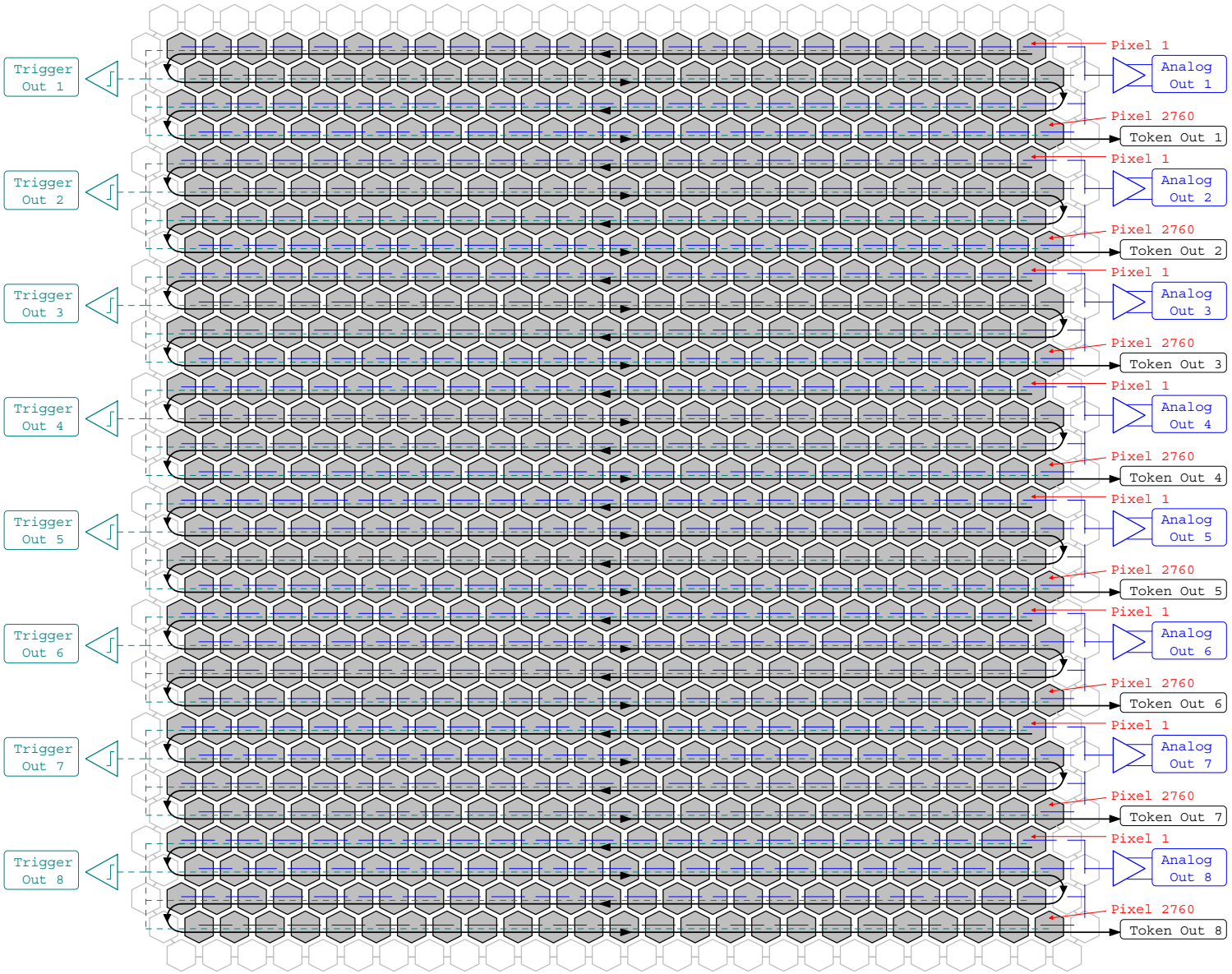

Figure 2: ASIC simplified pixel layout and serial readout architecture (actual number of pixels is larger than shown)

I/O Pin Description

I/O Name	Type	Function	Comment
VDD*	Supply	Positive supply terminal	Digital & ESD protection (pad ring) supply
VSS*	Supply	Negative supply terminal	Digital & Analog supply return (as well as substrate voltage)
AVDD*	Supply	Positive supply terminal	Positive supply for analog blocks (same voltage as applied to VDD pin)
Vring	Analog input	Guard ring potential	The active matrix is surrounded by a dummy pixel ring of 1 pixel width
Vtest	Analog input	Electrical & functional pixel test control	The charge injected is proportional to the voltage difference between Vtest and VSS pins
IntRef[0:3]	Analog output	Internal reference voltages	"IntRef0" is to be measured for the purpose of giving the correct value to the voltage applied to analog input "TrigRef". Acceptable load is min 1MΩ and max 100pF to ground
BiasOAn BiasOAp	Analog output	Internal bias voltage monitoring & decoupling	Decoupling capacitances of 1-10nF between "BiasOAn" and VSS and between "BiasOAp" and AVDD should be foreseen on the PCB
BiasN[1:4] BiasP[1:3]	Analog output	Internal bias voltage check	Provided for test only
TrigRef	Analog input	External reference voltage for self-triggering function	The DC voltage to be applied to "TrigRef" should match the internally-generated voltage available on pin "IntRef0" +/-50mV
Reset	5V-tolerant TTL input	Readout shift register initialization	Clears the content of the serial readout shift register & preloads the token for readout
CK	5V-tolerant TTL input	Shift register clock	All 8 clusters share the same clock. Tokens are shifted one cell forward at the falling edge of the register clock CK
RegFill	5V-tolerant TTL input	Allows more than 1 token in the register	Normally set to LOW for readout, can be maintained HIGH during several CK pulses for simultaneous write on several pixels
EnSelfTrig	5V-tolerant TTL input	Enable self-triggering function	Peak & Hold mode is activated by internal trigger or external "MaxHold" control, whichever comes first (EnSelfTrig=HIGH), or by external "MaxHold" only (EnSelfTrig=LOW)
EnTrigOut	5V-tolerant TTL input	Allows the monitoring of the self-triggering function	Set to "HI" for debugging purposes only: to avoid noise & crosstalk during data acquisition, "EnTrigOut" is normally set to LOW
MaxHold	5V-tolerant TTL input	Peak & hold mode control	Triggers the shaper's peak & hold mode
AnaReset	5V-tolerant TTL input	Analog memory reset	Resets analog memory of all pixels by setting the shaper back in normal (track) mode
Read	5V-tolerant TTL input	Selects readout mode	Connects the selected pixel output to analog bus
Write	5V-tolerant TTL input	Electrical pixel test control	At the rising edge of the Write signal, a charge is injected into the pixel selected with the serial data register
Vcm[1:8]	Analog input	DC common-mode voltage	1.5V typ. from the ADS5270. Can be set independently for each cluster to accommodate possible offsets
Out[1:8]+ Out[1:8]-	Analog outputs	Differential analog buffer outputs	Driving capability: +/-1V differential into 20pF to ground and 600Ω to "VCM"

I/O Name	Type	Function	Comment
Probe[1:8]	Analog output	Monitors the self-trigger analog signal	The self-trigger shaped analog pulse can be observed on the a scope with min 1MΩ and max 100pF to ground
TokenOut[1:8]	TTL output	Serial register output data	Flags readout of last pixel of each cluster
Ctrig[1:8]	Analog passive	Connection for external grounded capacitors	The self-triggering functions requires one grounded 100nF capacitance for each cluster
Threshold[1:8]	Analog input	Sets self-triggering threshold	Can be set individually for each cluster
TrigOut[1:8]bar	TTL output	Cluster self-trigger output	Goes to LOW state when an event exceeds the threshold within the cluster. Remains HIGH if “EnTrigOut”=LOW

*Note: these pins are present more than once around the chip. It is recommended to connect all pins sharing a common name to the same voltage source to insure the uniformity of power distribution inside the active matrix.

I/O Pin Assignment

The PGA256 pin ID/locations are given below according to their coordinates identified in Figure 3.

Pin name	Pin ID	Pin name	Pin ID	Pin name	Pin ID	Pin name	Pin ID
Probe1	A1	Ctrig1	D4	Threshold1	C2	AVDD	D3
VSS	B1	VDD	E4	TrigOut1bar	D2	VSS	E3
Probe2	C1	Ctrig2	F4	Threshold2	E2	AVDD	F3
VSS	D1	VDD	G4	TrigOut2bar	F2	VSS	G3
Probe3	E1	Ctrig3	H4	Threshold3	G2	AVDD	H3
VSS	F1	VDD	J3	TrigOut3bar	H2	VSS	J4
Probe4	G1	Ctrig4	J2	Threshold4	H1	AVDD	K3
VSS	J1	VDD	K4	TrigOut4bar	K1	VSS	K2
Probe5	L1	Ctrig5	L2	Threshold5	M1	AVDD	L4
VSS	N1	VDD	L3	TrigOut5bar	N2	VSS	M2
Probe6	P1	Ctrig6	M4	Threshold6	P2	AVDD	M3
VSS	R1	VDD	N3	TrigOut6bar	R2	VSS	N4
Probe7	T1	Ctrig7	P3	Threshold7	T2	AVDD	R3
VSS	U1	VDD	P4	TrigOut7bar	U2	VSS	T3
Probe8	V1	Ctrig8	R4	Threshold8	V2	AVDD	U3
VSS	W1	VDD	T4	TrigOut8bar	W2	VSS	V3
VSS	Y1	SelfTrig	U4	VDD	W3	EnTrigOut	V4
MaxHold	Y2	AnaReset	U5	EnSelfTrig	W4	VSS	V5
VSS	Y9	CK	U10	Write	Y10	Read	W10
Reset	Y11	VDD	W11				
RegFill	Y19	VDD	U16	VSS	W19		
VSS	Y20	TokenOut8	U17	VDD	V19	VSS	U18
AVDD	W20	Out8-	T17	Vcm8	U19	Out8+	T18
VSS	V20	TokenOut7	R17	VDD	T19	VSS	R18
AVDD	U20	Out7-	P17	Vcm7	R19	Out7+	P18
VSS	T20	TokenOut6	N17	VDD	P19	VSS	N18
AVDD	R20	Out6-	M18	Vcm6	N19	Out6+	M17
VSS	P20	TokenOut5	M19	VDD	N20	VSS	L18
AVDD	M20	Out5-	L17	Vcm5	L20	Out5+	L19
VSS	K20	TokenOut4	K19	VDD	J20	VSS	K17
AVDD	H20	Out4-	K18	Vcm4	H19	Out4+	J19
VSS	G20	TokenOut3	J17	VDD	G19	VSS	J18
AVDD	F20	Out3-	H18	Vcm3	F19	Out3+	H17
VSS	E20	TokenOut2	G18	VDD	E19	VSS	F18
AVDD	D20	Out2-	G17	Vcm2	D19	Out2+	E18
VSS	C20	TokenOut1	F17	VDD	C19	VSS	D18
AVDD	B20	Out1-	E17	Vcm1	B19	Out1+	C18
VSS	A20	AVDD	D17	BiasOAp	B18	BiasOAn	C17
BiasP1	A19	BiasP2	D16	BiasP3	B17	BiasN1	C16
BiasN2	A18	BiasN3	D15	BiasN4	B16		
VSS	C14	AVDD	A16	VSS	D12	AVDD	A14
Vtest	B11	VSS	A10	AVDD	B10		
VSS	A6	AVDD	C8	AVDD	A3	Vring	D6
IntRef3	B3	IntRef2	C4	IntRef1	A2	IntRef0	D5
TrigRef	B2	VSS	C8				

Table 1: I/O pin assignment

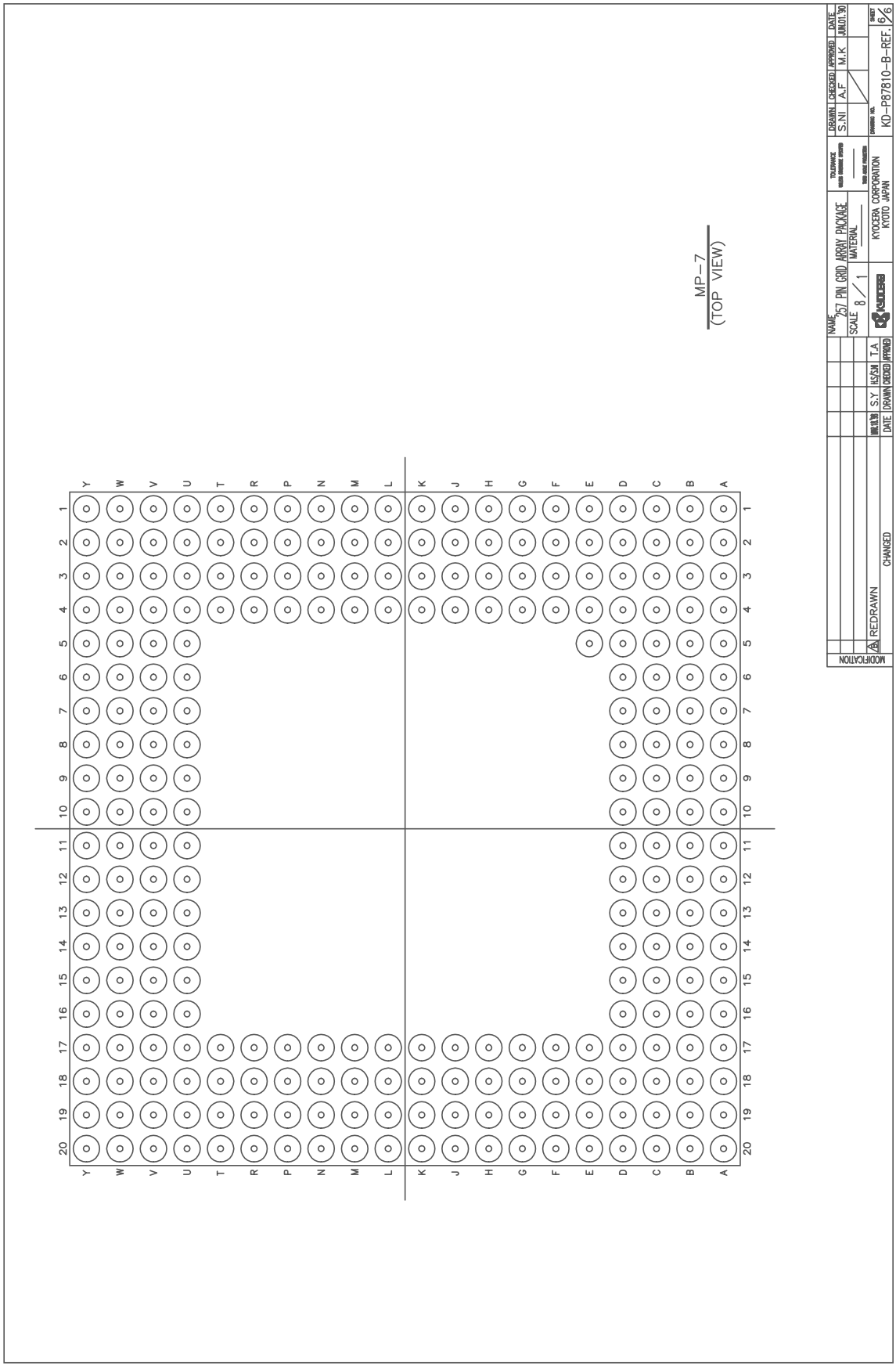

Figure 3: PGA256 pin grid array coordinates

Pixel Event Readout

Architecture

Each cluster includes its own self-triggering function, in which a replica of all 2760 CSA's outputs are summed and shaped before being discriminated against an externally adjustable level set on pin "[Threshold[1:8]". The shaping requires a 100nF external capacitor to ground (VSS) at each of the "Ctrig[1:8]" pins. The common reference level "Ref" for the 8 self-trigger shapers is applied externally such as to match an internal reference voltage available for precise evaluation on pin "IntRef0". The shaped output waveform is available for test purposes on the "Probe[1:8]" pins.
The peak detection and subsequent hold mode is initiated either with an external pulse on the "MaxHold" input or, if "EnSelfTrig" is set to HIGH, from the internal trigger signal built by wired-OR combination of the self-trigger output of each cluster, which can be observed on the digital outputs "TrigOut[1:8]bar".
The hold mode is terminated when a pulse is applied to the "AnaReset" input, in which case all pixels of the matrix return to the track mode simultaneously.

Timing Characteristics

VDD-VSS ≥ 3.0V unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
Tpk	Shaper peaking time	3	4	5	us
Tdh	Delay between incoming event & rising edge of MaxHold	0		2	us
Tmh	MaxHold pulse width	1		Tstore	us
Tpd	Peak detection mode duration	10		20	us
Tstore	Analog data retention time for a drift during hold mode lower than 0.1fC equivalent input charge)	1			ms
Tar	AnaReset pulse width	1			us
Tr	Analog memory recovery time after hold			100	us

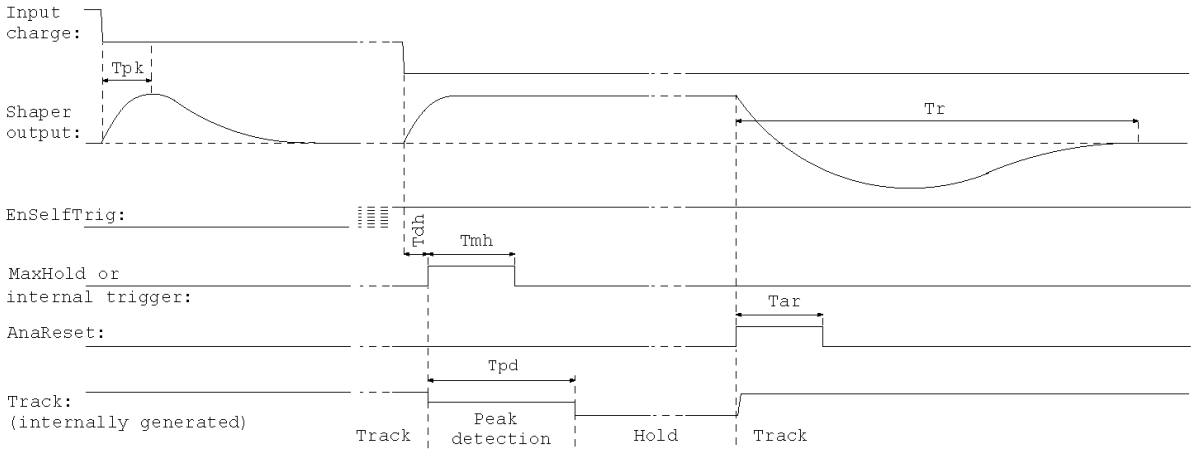

Figure 4: Pixel event readout timing definition

Serial Output Interface

Architecture

There are 8 identical clusters sharing the same digital readout control signals “Reset”, “CK” & “Read” (Figure 2). This means that all clusters are read in parallel and that the analog data at the balanced outputs “Out[1:8]+” & “Out[1:8]” correspond to information stored in pixels having the same relative position in their respective clusters.
Each pixel includes a register element (Figure 1), chained with the previous and next pixels as sketched in Figure 2. At the beginning of the chain (before pixel labeled #1) there is an additional register element (hereafter called #0). The latter is preloaded with the token when a pulse is applied to the “Reset” input. At the falling edge of the first clock pulse after reset the token activates pixel #1 register element and it propagates one element further at each subsequent clock pulse, until it appears to the “TokenOut” output when the last pixel is activated. The action of setting input “Read” HIGH simply connects the analog output of the pixel hosting the token to the buffered analog output.
During the readout process the input “RegFill” is to be held LOW because, within each cluster, only one pixel at a time can be connected to the analog bus.

Timing Characteristics

VDD = AVDD = 3.3V , VSS = 0.0V, AGND = 0.5V, T_{amb} = 25°C unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
Tr1	Reset HIGH duration before initiating read sequence	100			ns
Tdck	Delay between falling edge of Reset and rising edge of first clock pulse	20			ns
Tck	Input clock period	100			ns
Tck0	Input clock LOW duration	50			ns
Tck1	Input clock HIGH duration	50			ns
Trf	Input clock rise/fall time			10	ns
Trd1	Delay between rising edge of Read and falling edge of related CK for read	0			ns
Trd0	Delay between falling edge of Read and falling edge of last CK for read	Tck			s
Tasu	Analog buffer output setup time (CL < 20pF[1])			100	ns
Tahd	Analog buffer output hold time (for less than 1mV drift)			1	ms

Note [1]: It is recommended to minimize the loading capacitance of the on-chip high-speed analog output buffer. Capacitance larger than 20pF may increase the settling time and ultimately lead to instability.

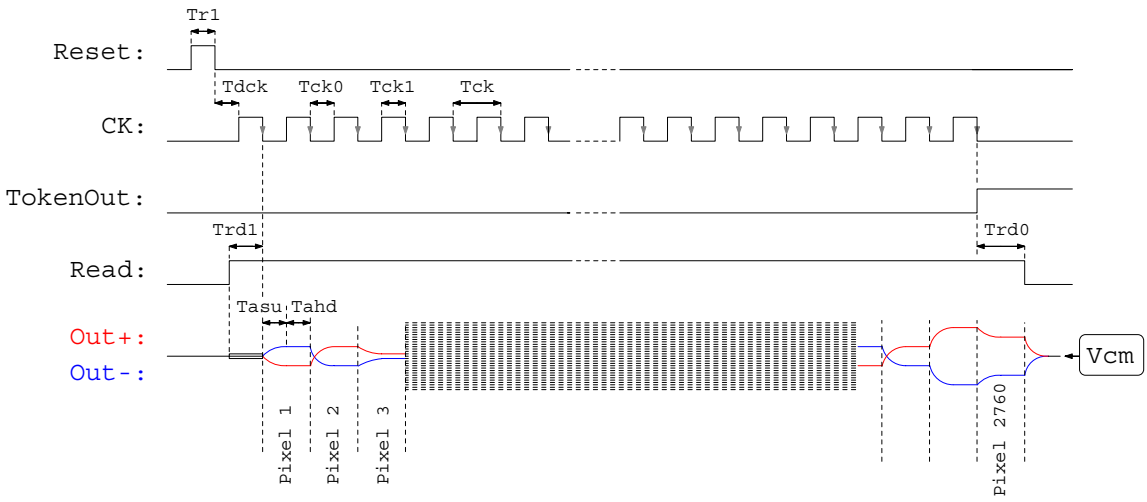

Figure 5: Serial output interface timing definition

Pixel Electrical Test

After a general reset pulse, pixel #N of any cluster is selected for write/read by sending N clock pulses as described above. Then it can be stimulated electrically at the rising edge of the “Write” signal. The injected charge -Qin is proportional to the voltage difference between pin “Vtest” and VSS supply (ΔQin = 10fC/V typ.). Keeping the “Read” input high, the shaped pulse of the selected pixel can be observed simultaneously at the analog output as long as both the “MaxHold” and the “EnSelfTrig” inputs are LOW. Additionally, if the “MaxHold” input is raised no later than 2 us after the rising edge of the “Write” signal, the peak-and-hold operation can be monitored in real time. The pixel is then put back in normal shaping mode after applying a pulse on the “AnaReset” input.
Note that the readout architecture of the circuit allows only one pixel at a time on each cluster to be monitored in real time, i.e. to be connected to the analog bus for read while stimulated with the write command.
Alternately, several pixels on each cluster can be stimulated at once (simultaneously) by feeding the readout register with more than one token: this is accomplished by holding the “RegFill” input HIGH for several clock cycles (in addition to the token already present in register element #0 after reset, every clock pulse applied when “RegFill” is HIGH will push another token into register element #0 while shifting the word one pixel forward into the chain). In this case the “Read” input must be kept LOW when the “Write” signal is activated. The “MaxHold” signal is to be raised simultaneously or no later than 2us after “Write”. The information stored in each pixel can then be read out normally (one by one) after resetting the register.

Electrical Characteristics

VDD = AVDD = 3.3V , VSS = 0.0V, AGND = 0.5V, T_{amb} = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Idd	Total supply current	3.0V<VDD-VSS<3.6V no load on analog outputs (Iout = 0)			500	mA
V(Out+) V(Out-)	Analog output voltages	Vcm = 1.5V	VSS +0.5		VDD -1.0	V
Ro	Analog output impedance [1]	1V < V(Out+) < 2V 1V < V(Out-) < 2V			5	Ω
Qin	Input signal		0.2		20	fC
INL	Integral non-linearity				0.5	fC
A	Average input sensitivity	ΔV(Out+,Out-)/ΔQin	70	90	110	mV/fC
dA	Pixel-to-pixel gain variation				5	%
OS	Average DC offset		-1	0	1	fC
dOS	Pixel-to-pixel offset variation		-1		1	fC
Tpk	Shaper peaking time		3	4	5	us
Trc	Recovery time after hold				100	us
ENC	Equivalent input noise charge				200	e^-
V(IntRef0)	Internal reference	3.0V<VDD-VSS<3.6V	850	930	1000	mV
V(TrigRef)	External reference voltage for self-triggering function	to be set to V(IntRef0) within ±50mV	850		1000	mV
V(Threshold)	Self-triggering threshold	Defined wrt. V(TrigRef)	50			mV
Strig	Self-triggering threshold sensitivity	V(Threshold,TrigRef)/ ΔQtot (on cluster)		20		mV/fC
Stest	Analog test input sensitivity	ΔQin / (Vtest –VSS)	8	10	12	fC/V
Vring	Externally applied guard ring potential wrt. VSS	V(Vring,VSS)	500	550	600	mV

Note [1]: The on-chip analog output buffer is able to drive a 600Ω (or more) load connected to the common-mode voltage defined by the external voltage applied to Vcm pin.