VLSI Readout ASIC for MPGD

General Description

This ASIC constitutes the multiple anode of the **M**icro**P**attern **G**as **D**etector. The CMOS VLSI chip integrates more than 16.5 million transistors and is organized as a 15mm x 15mm active area of 105'600 pixels. Each pixel is composed of a hexagonal electrode (top layer of metal) connected to a charge-sensitive amplifier followed by a shaping circuit. The chip's honeycomb matrix is organized in 16 identical clusters of 6600 pixels (22 rows of 300 pixels each) with an independent differential analog readout buffer. Each cluster also features customizable self-triggering capability. Upon the activation of an external digital control input, or from on-chip wired-OR combination of each cluster self-triggering circuit, the maximum of the shaped pulse is stored inside each pixel cell for subsequent readout. The latter is accomplished by sequentially connecting the output of each cell to the analog bus common to each cluster. The self-triggering function also includes an on-chip signal processing for automatic localization of the event. This allows reducing the readout time, as in the corresponding readout mode only the pixels within the region of interest are scanned.

Features

Pixel:

- shaping time: 3-10us (externally adjustable)
- full-scale linear range: FS = 5fC (30ke-)
- line/column addressing
- electrical stimulation for test purposes

Matrix organization:

- 300 (width=300x50um=15mm) x 352 (height=352x43.3=15.24mm) pixels
- 16 clusters of 300 x 22 = 6600 pixels each or 8 clusters of 300 x 44 = 13200 pixels each

Trigger:

- user-selectable internal/external

Internal trigger functionality:

- every 4 pixels (1 mini-cluster) contribute to a local trigger with a dedicated shaping amplifier
- each pixel includes a masking function to disable its contribution to the trigger function
- threshold: < 3000e- (10% of FS
- each of the 16 clusters' trigger level is defined independently to accommodate possible "region" offset
- the event is localized in a rectangle containing all triggered mini-clusters plus a user-selectable margin of 10 or 20 pixels (0.5mm or 1.0mm)
- the chip calculates the resulting area of interest defined with coordinates (Xmin,Ymin) & (Xmax,Ymax) corresponding to the upper-left & lower-right corners, respectively

Readout:

- **Read mode 0** (direct addressing): the pixel is selected with its (X,Y) coordinates by entering its column (X) & line (Y) index binary code. This is the preferred readout mode during the electrical test of a single pixel.
- **Read modes 1 & 2** (standard readout): sequential within each cluster (line-by-line from top left down to bottom right), all 8 (mode 1) or 16 clusters (mode 2) read out in parallel (1 buffer amplifier per cluster).
- **Read mode 3** (advanced readout): sequential within the area of interest defined by coordinates (Xmin,Ymin) & (Xmax,Ymax).

Specificity of mode 0:

- 2x9-bit Xaddr[8:0],Yaddr[8:0] to directly address one single pixel anywhere on the matrix

Specificity of modes 1 & 2:

- target readout time: 660/1320us (100ns per pixel) for 8/16 clusters
- sequential readout of pixels within each cluster through line/column addressing
- left-to-right column shift register with 1 recirculating token driven by the master clock for column addressing
- top-down shift register with 8/16 tokens (for 8/16 clusters) for line addressing, driven by the column address token
- the “Read” control input is used to initialize all readout registers with the required tokens

Specificity of mode 3:

- only available in conjunction with the internal trigger operation
- the user-selectable margin of 10 (MarginHi=0) or 20 pixels (MarginHi=1) is added to the minimum rectangle area containing all triggered mini-clusters and the result is used to enter the line & column tokens at the right place to scan the corresponding area of interest as one dynamically-defined cluster
- the corresponding coordinates (Xmin,Ymin) & (Xmax,Ymax) are available as four 9-bit data outputs as soon as the analog data acquisition process following an internally triggered event has terminated, flagged by the “DataReady” output

Electrical test:

- **Write mode 0** (one pixel at a time): the pixel is selected with its (X,Y) coordinates by entering its column (X) & line (Y) index binary code. The shaped signal can be monitored in real time together with read mode 0.
- **Write modes 1 or 2**: write all odd or all even columns at once.
- **Write mode 3**: write all pixels simultaneously.
- the amount of charge injected to each pixel is set by the DC level Vtest (common to the whole matrix)
- the stimulus occurs at the rising edge of "Write" (LVDS input)

Masking function:

- the trigger contribution of any pixel can be disabled by direct addressing (the pixel address is entered with **Read mode 0 & Write mode 0**)
- the masking bits are to be set at each power-up of the circuit

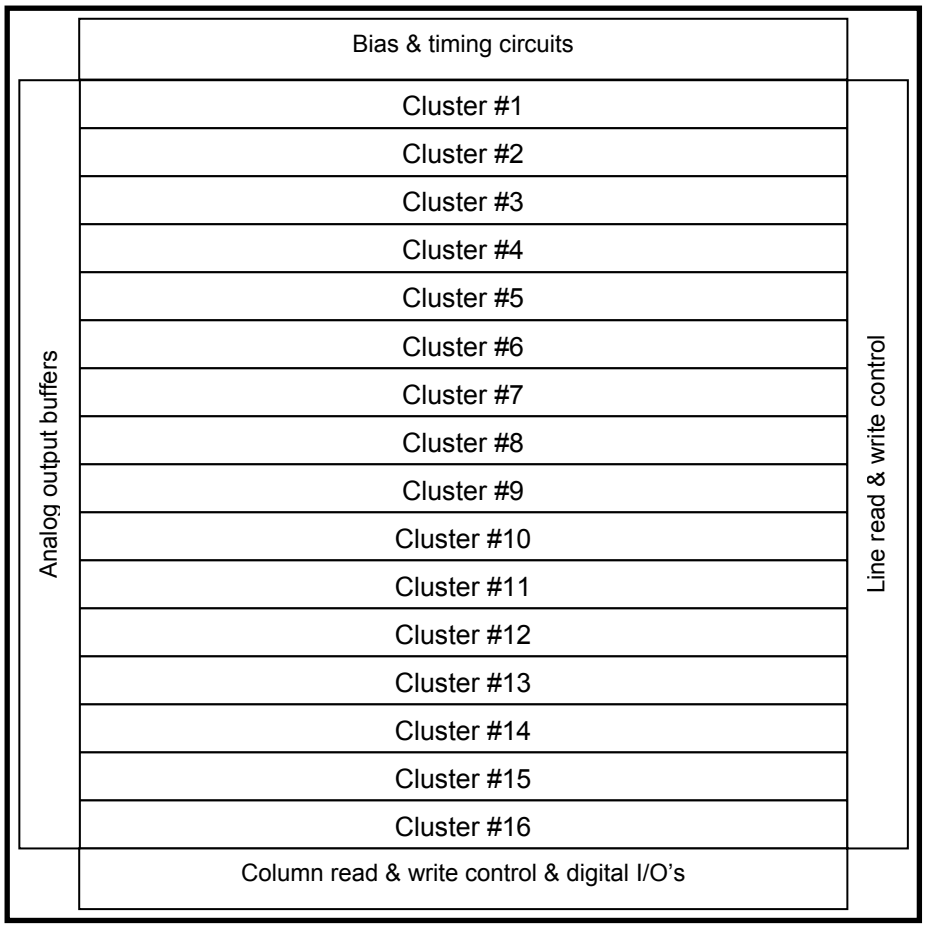
Analog outputs:

- balanced output buffer (+/-1V) compatible with TI ADC ADS572x.
- read mode 1, respectively 2 & 3 uses 8, respectively 16 & 1 analog buffer(s)
- unused buffers are disabled to minimize power consumption

Digital controls:

- a common TTL-compatible serial interface is used both to configure the chip and enter any (X,Y) address and to read out the impact rectangle coordinates (Xmin,Ymin) & (Xmax,Ymax)
- external digital controls to be applied within the analog data acquisition timeframe (Write, TrigWindow, MaxHold) or analog readout process (Read, CK) use LVDS interfaces
- internally generated trigger given as output for time stamp (TrigOut) is also LVDS

Chip Architecture & Layout



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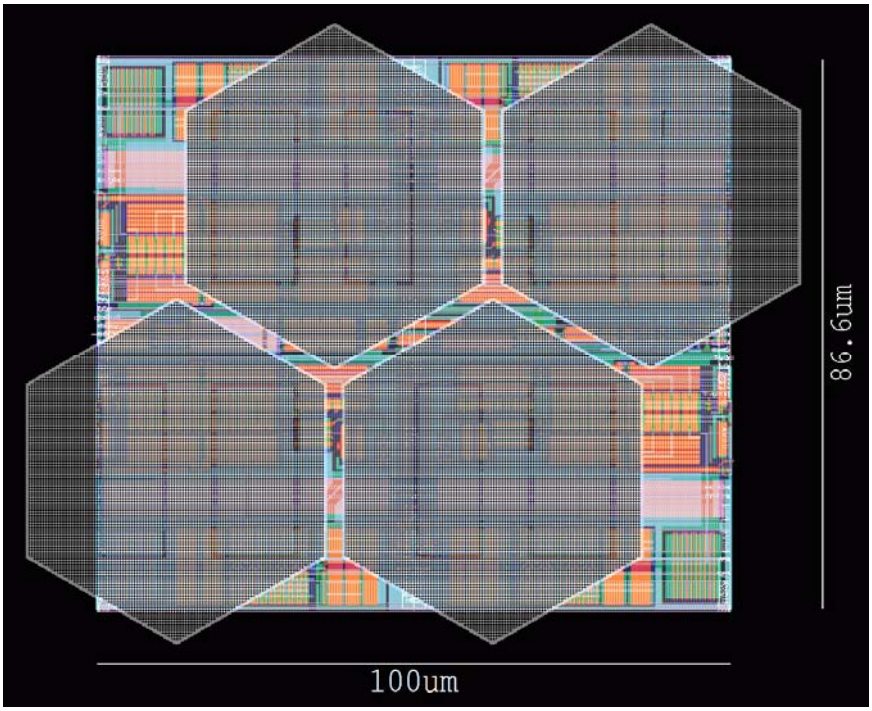

Layout of 4 pixels with local trigger (1 mini-cluster)

I/O Pin Description

I/O Name	Type	Function	Comment
VDDH*	Supply	3.3V supply terminal	Digital & ESD protection (pad ring) supply
VDD*	Supply	1.8V supply terminal	Supply of core digital circuits
VSS*	Supply	Supply return	Digital supply return (as well as substrate voltage)
AVDDH*	Supply	3.3V supply terminal	Supply of analog peripheral blocks (same voltage as applied to VDDH pin)
AVDD*	Supply	1.8V supply terminal	Supply of core analog blocks (same voltage as applied to VDD pin)
AVSS*	Supply	Supply return	Analog supply return (as well as substrate voltage)
LdDefConf	TTL input	Default configuration	Loads default values for configuration & address bits (RMode=00, WMode=00, EnSelfTrig=0, MarginHi=0, Xaddr=511, Yaddr=511)
EnPixTrig	TTL input	Enables all pixels trigger contribution	Used to clear the disable register of all pixels
Disable	TTL input	Masks selected pixel for internal trigger	Disable trigger contribution of pixel selected by Xaddr[8:0] & Yaddr[8:0] Both “WMode” & “Rmode” are to be set to 00 for this operation
Write	LVDS input#	Electrical pixel test control	At the rising edge of the Write signal, a charge is injected into the selected pixel(s) according to the write mode set by “WMode”
Vtest	Analog input	Electrical & functional pixel test control	The charge injected is proportional to the voltage difference between Vtest and AVSS
Threshold[1:16]	Analog input	Sets self-triggering threshold	Can be set individually for each cluster. Defined with respect to internal analog reference voltage “Ref0”
TrigWindow	LVDS input#	Internal trigger gating	Enables/disables threshold comparator (e.g. to avoid false triggering during analog signal recovery following an analog reset)
MaxHold	LVDS input#	Peak & hold mode control	Triggers the shaper’s peak & hold mode in external trigger mode
TrigOut	LVDS output#	Internal trigger	Only available in self-triggering mode (EnSelfTrig = 1)
DataReady	TTL output	Indicates end of data acquisition process	Validates the current Xmin,Ymin, Xmax & Ymax data and prompts for readout
Read	LVDS input#	Initiates readout mode	Connects the selected pixel output to analog bus
CK	LVDS input#	Readout column register clock	The column index is incremented at the falling edge of CK
EndRO	TTL output	Flags end of readout process	Available for Rmode = 01, 10 and 11
AnaReset	TTL input	Analog memory reset	Resets analog memory of all pixels by setting the shaper back in normal (track) mode and resets the trigger latch of each mini-cluster.
Out[1:16]+ Out[1:16]-	Analog outputs	Differential analog buffer outputs	Driving capability: +/-1V differential into 20pF to ground and 600Ω to “VCM”
VCM	Analog input	DC common-mode voltage of analog buffers	1.5V typ. From the ADS527x. Common to all clusters.

I/O Name	Type	Function	Comment
SDin	TTL input	Serial data input	The serial-parallel interface (SPI) is a simple FIFO register. Input data is sampled at the falling edge of SCK. Output data changes at the rising of SCK.
SDout	TTL output	Serial data output	
SCK	TTL input	Serial data clock	
LoadConf	TTL input	Load configuration	Bits in the SPI register are copied into the configuration register upon applying a pulse on “LoadConf” input
LoadAddr	TTL input	Load XY address	Bits in the SPI register are copied into the XY address register upon applying a pulse on “LoadAddr” input
ReadConf	TTL input	Read configuration	Bits in the configuration register are copied into the SPI register upon applying a pulse on “ReadConf” input
ReadMinMax	TTL input	Read XY min & max of readout rectangle	Bits in the XYminmax register are copied into the SPI register upon applying a pulse on “ReadMinMax” input
Ref[0:4]	Analog	Internal reference voltages	Internal analog reference “Ref0” is provided for the purpose of giving the correct value to the voltage applied to analog input “Threshold”. Acceptable load is RL>10MΩ and CL<100pF
Vxyz	Analog	Internal bias current or voltage monitoring	Several access points to internal bias for capacitive decoupling and/or fine-tuning of specific analog performance (gain, shaping time, speed, hold delay etc…)

Notes:

* these pins are present more than once around the chip. It is recommended to connect all pins sharing a common name to the same voltage source to insure the uniformity of power distribution inside the active matrix.

for convenience, LVDS inputs & outputs use external termination resistors and are able to operate in TTL-compatible mode:

- for inputs: remove the termination resistor and drive the non-inverting input with the TTL signal while the inverting input terminal is tied to a mid-point (e.g. VSS+1.5V)
- outputs: can be used as an open-drain together with an external pull-up resistor.

Electrical Characteristics

VDD=AVDD=1.8V, AVDDH=3.3V VSS=AVSS=0.0V,, T_{amb} = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Ptot	Total power dissipation		400		800	mW
V(Out+) V(Out-)	Analog output voltages	Vcm = 1.5V	VSS +0.5		VDD -1.0	V
Ro	Analog output impedance [1]	1V < V(Out+) < 2V 1V < V(Out-) < 2V			5	Ω
Qin	Input signal		0.05		5	fC
INL	Integral non-linearity				0.1	fC
A	Average input sensitivity	∆V(Out+,Out-)/∆Qin	320	400	480	mV/fC
dA	Pixel-to-pixel gain variation				5	%
OS	Average DC offset		-0.2	0	0.2	fC
dOS	Pixel-to-pixel offset variation		-0.2		0.2	fC
Tpk	Shaper peaking time	without adjustment	3	4	5	us
Trc	Recovery time after hold				50	us
ENC	Equivalent input noise charge				200	e^-
Strig	Self-triggering threshold sensitivity	V(Threshold,Ref0)/ ∆Qtot (on 1 mini-cluster)		200		mV/fC
Stest	Analog test input sensitivity	∆Qin / (Vtest –VSS)	8	10	12	fC/V

Note [1]: The on-chip analog output buffer is able to drive a 600Ω (or more) load connected to the common-mode voltage defined by the external voltage applied to VCM pin.