Characterization of the HEFT CdZnTe pixel detectors

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ABSTRACT

We have developed large format CdZnTe pixel detectors optimized for astrophysical applications. The detectors, designed for the High Energy Focusing Telescope (HEFT) balloon experiment, each consists of an array of 24×44 pixels, on a 498 μm pitch. Each of the anode segments on a CdZnTe sensor is bonded to a custom, low-noise application-specific integrated circuit (ASIC) optimized to achieve low threshold and good energy resolution. We have studied detectors fabricated by two different bonding methods and corresponding anode plane designs—the first detector has a steering electrode grid, and is bonded to the ASIC with indium bumps; the second detector has no grid but a narrower gap between anode contacts, and is bonded to the ASIC with conductive epoxy bumps and gold stud bumps in series. In this paper, we present results from detailed X-ray testing of the HEFT pixel detectors. This includes measurements of the energy resolution for both single-pixel and split-pixel events, and characterization of the effects of charge trapping, electrode biases and temperature on the spectral performance. Detectors from the two bonding methods are contrasted.

Keywords: CdZnTe radiation detectors, conductive epoxy, flip-chip devices, indium bump-bonding, radiation detector circuits, sample and hold circuits, semiconductor device bonding, X-ray astronomy detectors

1. INTRODUCTION

We have developed large format CdZnTe hybrid pixel detectors optimized for use as focal plane detectors for hard X-ray telescopes. The detectors are designed for the High Energy Focusing Telescope (HEFT)[1] balloon experiment, and are optimized to achieve good spectral resolution with low power over the energy range 5–100 keV. Each HEFT detector consists of an array of 24×44 pixels on a 498-μm pitch. Each pixel is bonded to its own amplifier circuitry on a custom, low-noise application-specific integrated circuit (ASIC). We have investigated both indium bump bonding as well as gold stud-epoxy bonds, and we compare detectors fabricated using each.

In this paper, we first describe the detector geometry for two different sensor architectures that we have investigated. Next, we discuss the data processing steps we take to obtain spectra out of the signals from the detector hardware. Finally, we characterize the performance of the two different detector achitectures in terms of its spectral resolution, efficiency and other properties.

2. SYSTEM CONFIGURATION AND DETECTOR GEOMETRY

The HEFT detector system consists of a CdZnTe-ASIC hybrid detector, an analog-to-digital converter (ADC) for the ASIC output, a microprocessor to operate the ASIC, and support electronics. Figure 1 shows a diagram of the detector system. We describe the relevant components in details in this section.

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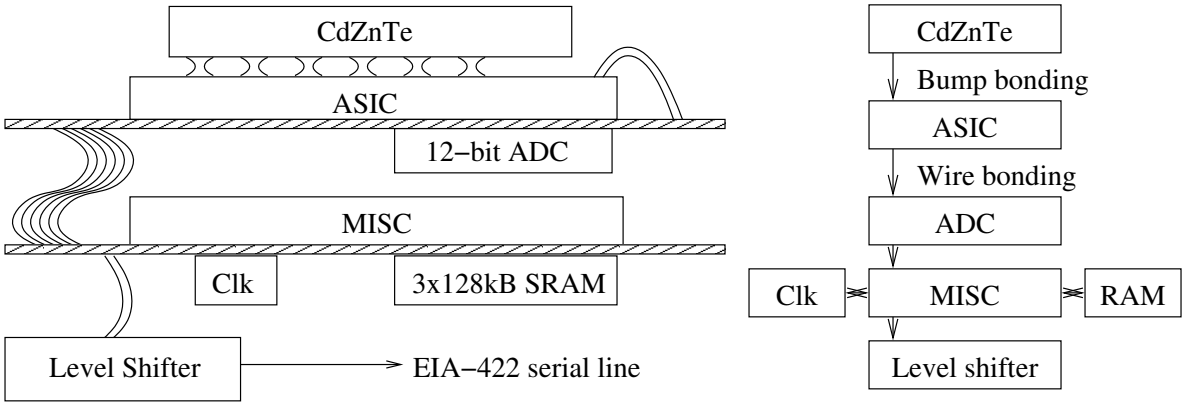

Figure 1. Diagram and flow chart of the detector system.

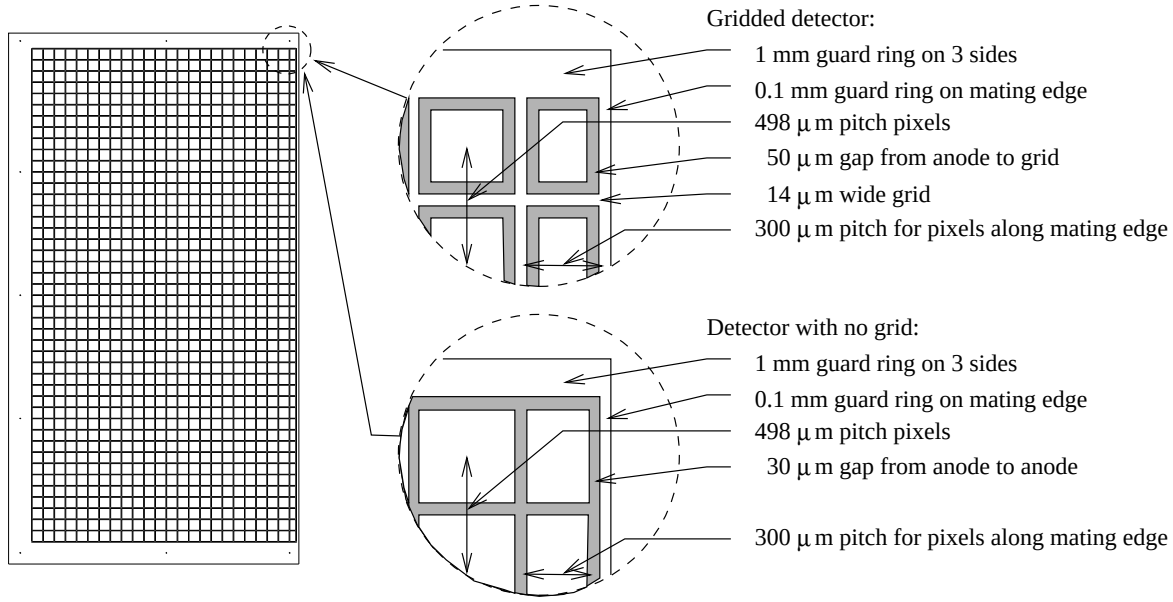

Figure 2. Anode plane patterns. The gridded pattern at the top is designed for indium bump bonding to minimize the anode contact size and input capacitance. The no-grid pattern at the bottom is designed for bonding with conductive epoxy and gold stud bumps, which are 4–5 times taller than indium bumps. Both patterns contain a mating edge, where the last row of pixels and the guard ring are contracted for a second detector to be placed side by side.

2.1. CdZnTe

We purchase CdZnTe crystals with platinum electrodes from eV Products. The size of the sensor is 23.6 mm by 12.9 mm by 2 mm thick. This was the maximum size available given specification of single-crystal, highly uniform material at the time of our first design. The cathode is a monolithic platinum contact, while the anode plane is patterned into a 24×44 pixel array of 498-μm pitch, surrounded by a guard ring that is 1 mm on three sides, and 0.1 mm on the fourth (so that two detectors can be placed side by side to form a roughly square sensor area with minimal dead area in between). Figure 2 shows two anode plane patterns we have used in different hybrids.

We have investigated two anode plane patterns, one with a shaping electrode, or grid in between pixel contacts,[2] and one with larger pixel contacts, and a 30 μm gap in between. These two anode plane patterns accommodate the two bonding methods we use to connect the CdZnTe to the ASIC. The CdZnTe sensors with the gridded anode pattern are indium bump-bonded to ASICs. These indium bumps are only 8–10 μm tall, requiring us to reduce the anode contact size to minimize input capacitance. Because of the larger gap between contacts, we add a grid, held at a potential intermediate between the cathode and anode to steer charge hitting the surface between pixels toward the anode, minimizing charge loss in the gap. A different bonding approach, which we have adopted for all future sensors, affords a larger CdZnTe to ASIC separation, enabling us to eliminate the grid, use larger contacts, yet maintain low input capacitance. The bonds consist of a series connection of conductive epoxy bumps (on the CdZnTe) and gold stud bumps (on the ASIC).[3] These connections are about 40 μm tall. In this paper, we present results from one hybrid of each of these architectures.

2.2. ASIC readout

We developed the custom ASIC at Caltech as part of the HEFT program. It consists of a 24×44 pixel array, also of 498-μm pitch, with the pixel pattern matching that on the CdZnTe anode plane. Each pixel is implemented with its own preamplifier, shaping amplifier, discriminator, and sampling and pulsing circuits. All pixels share a serial readout line. We designed the ASIC for low noise and power; it consumes about 50 mW of power under normal operation. We provide further details on the ASIC circuitry in Section 3.

2.3. Digital circuitry

A P24 microprocessor—a 24-bit Minimal Instruction Set Computer (MISC) implemented on an Actel A54SX72A FPGA to run Forth—controls the ASIC. The MISC runs on a 7.3728 MHz clock cycle, driven by a 14.7456 MHz oscillator chip. Three 128 kB SRAMs provide it with 128k of 24-bit memory. The output of the ASIC readout line is digitized by an 80 mW, 12-bit ADC12062. The MISC then pipes the digitized data out to an EIA-422 serial line via a level shifter. The entire detector system consumes about 700 mW of power.

3. READOUT CIRCUITRY—DESIGN DETAILS

3.1. Basic concepts

The design of the ASIC circuitry is the key to achieving low power, low noise and good spectral resolution. In order to achieve low power, we have chosen a design that is different from the conventional amplifier chain. In our design, the signal shaping and peak detection stages of the conventional chain are replaced by a bank of 16 switch capacitors arranged to continuously capture successive samples of the preamplifier output. The result is a large reduction in power dissipation—from 250 μW to 50 μW per pixel—while allowing off-chip digital signal processing to extract near optimal energy resolution.

3.2. Implementation

The implementation of the sample and store mechanism with a bank of 16 capacitors is illustrated in Fig. 3. The preamplifer output is converted to a current and is integrated by the capacitors, cyclically one by one, with a 1 μs integration time. This process gives us a record of the current level during the previous 15–16 μs at any given time. When a trigger is detected, sampling continues for 8 more samples, after which the circuit freezes while the samples are read out.

In addition to reading out the 16 samples from each triggered pixel, we also read out samples from a collection of other pixels for additional information to help with the pulse height recovery process. These pixels include all the ones neighbouring any triggering pixel (ie, those sharing an edge or a corner with a triggering pixel), and a 3×3 array of reference pixels remote from the triggered pixels. Samples at the neighbouring pixels contain any systematic noise that is common in the vicinity of the triggering pixel, while samples at the reference pixels contain noise that is common to the entire chip. The neighbouring pixels may also have collected a small fraction of the charge induced from the X-ray event, if the event has occurred near the edge of the triggering pixel, and this charge may be too small to have triggered the neighbouring pixel. With these additional samples, we implement a second discriminator in software with a much lower threshold, and also remove systematic noise from the triggered pixels.

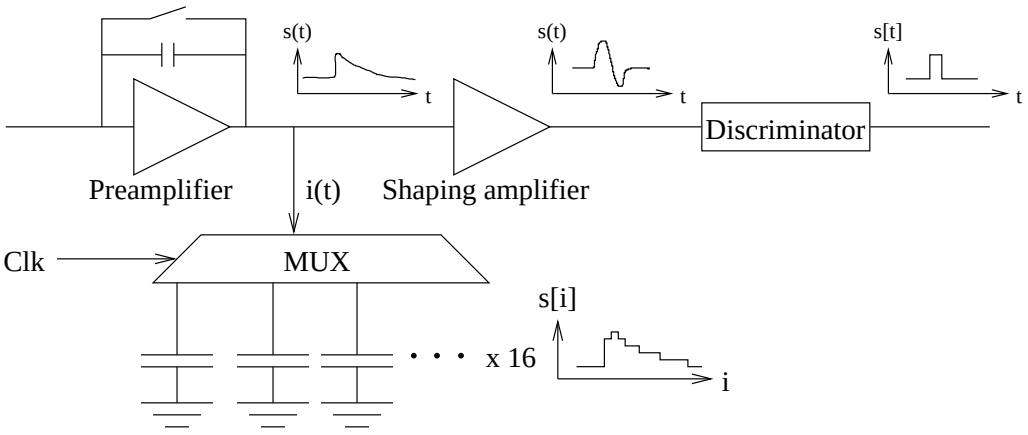

Figure 3. Illustration of the sample and store mechanism with a bank of 16 capacitors.

With this scheme, an event triggering a single pixel involves reading out 16 samples from $3\times3+3\times3 = 18$ pixels ($18 \times 16 = 288$ 12-bit numbers). An event where two adjacent pixels trigger (which we term a charge-sharing event) requires reading out 16 samples from $4 \times 3 + 3 \times 3 = 21$ pixels ($21 \times 16 = 336$ 12-bit numbers). With additional information (such as pixel coordinates, time information, etc), each event produces about 0.5 kbyte of information. The read out process takes about about 30 ms. As implemented for HEFT, with one ADC for two hybrid sensors, the focal plane can tolerate count rates of up to 100 counts/s before saturating.

4. SOFTWARE PROCESSING

With much signal processing delegated off-chip, software processing becomes an important procedure that determines the quality of pulse height recovery. The software processing sequence starts with a preliminary screening of the event record, which screens out abnormal events. In most of these abnormal events, there are either more than two triggering pixels, or two triggering pixels that do not share a common edge. Noise is the most common cause for these events. According to our previous detector modelling results,[4] we expect no more than 3% of all events to have charge shared amongst three or more pixels. The rate of having two photon events occuring within a single 1 μs integration period is also low. Other events that are screened out by this process includes the occasional (a few times in a million) occurrence of bad encodings, and events occuring too soon after a circuit reset, when the quiescent signal level has not been stabilized yet.

The next stage of processing involves the removal of systematic noise common to all pixels. We obtain the noise level as the average of samples measured at the nine reference pixels. For each of the 16 integration periods in an event record, the average noise level is subtracted from the samples measured at the triggering and neighbouring pixels. We then calculate a pulse height from each pixel that has a noise-corrected sample sequence, as the difference between the average of the last six samples and the average of the first six samples in the sequence. The pulse heights are then passed through a software discriminator, in search of charge-sharing events that are hidden from the hardware discriminator circuit by noise. Because the common noise has been removed, we are now able to set the threshold below 1 keV, as opposed to the hardware threshold near 8 keV. Events with false triggers are also eliminated at this stage.

For the single-pixel and two-pixel (charge-sharing) events that remain, we recalculate their pulse heights with a more sophisticated formula that takes the values of all 16 noise-corrected samples into account. Finally, the pulse heights are shifted and scaled to compensate for differences in amplifier gains and capacitor offsets across pixels. The pulse height pairs in charge-sharing events are summed, and all events are binned to produce spectra and other related information, which we present in the next section.

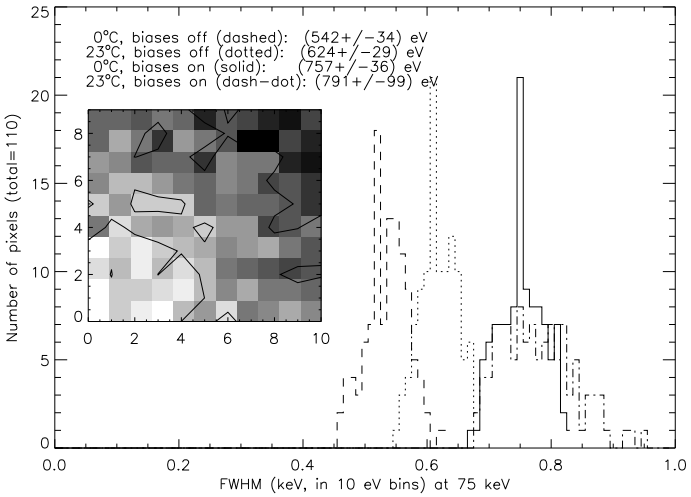

Figure 4. Distribution of electronic noise in a 11×10 pixel area of the gridded detector, at four different bias and temperature combinations. The inset map shows the spatial distribution of the same data, with brightness proportional to the noise magnitude.

5. DETECTOR CHARACTERIZATION

In this section, we present the detector performance under a range of temperatures and bias voltages for both architechtures: the grided detector with indium bumps, and the detector with no grid, bonded with epoxy studs. For practical reasons (to collect sufficient statistics in a reasonable time) we present detailed results from a contiguous area of 10×11 pixels.

5.1. Electronic noise

The intrinsic energy resolution of the detector hybrid at low X-ray energies is predominantly determined by the electronic noise in the ASIC circuitry. We measure the electronic noise as the full width at half maximum (FWHM) of a Gaussian spectral line produced by electronic pulses with energies equivalent to 75 keV photons. The distribution of electronic noise for the gridded detector is shown in Fig. 4.

5.1.1. Temperature dependence

The dotted and dashed lines in Fig. 4 show the distributions of the electronic noise for 110 pixels, at room temperature ($\approx 22^oC$) and at 0^oC, respectively, when all electrode biases are set to zero. Zero bias ensures that we are measuring the noise component from the electronics itself, rather than shot noise caused by leakage current through the CdZnTe crystal that is channelled into the preamplifier inputs. At room temperature, our ASIC design has an energy resolution of (624 ± 29) eV FWHM at 75 keV, due to thermal noise in the circuitry; at 0^oC, jitter in the circuitry decreases, and the resolution is improved slightly to (542 ± 34) eV FWHM at 75 keV. If pulses at these pixels are all summed together, the resulting 75-keV line has a FWHM of 623 eV at room temperature and 540. eV at 0^oC.

5.1.2. Leakage current contribution

For the grided detector, leakage current is introduced by surface leakage between the grid and contact, as well as by bulk leakage. The magnitude of the contribution depends on the surface and bulk resistivities, which vary from detector to detector, and the operating bias voltage. For the grided hybrid evaluated here, when the biases are set to nominal values of -300 V at the cathode and -4 V at the steering electrode grid, both relative to the anodes, noise is introduced by surface leakage current, and the resolution degrades to (791 ± 99) eV at room temperature and (757 ± 36) eV at 0^oC. The resolutions in the summed spectra are 779 eV and 756 eV FWHM,

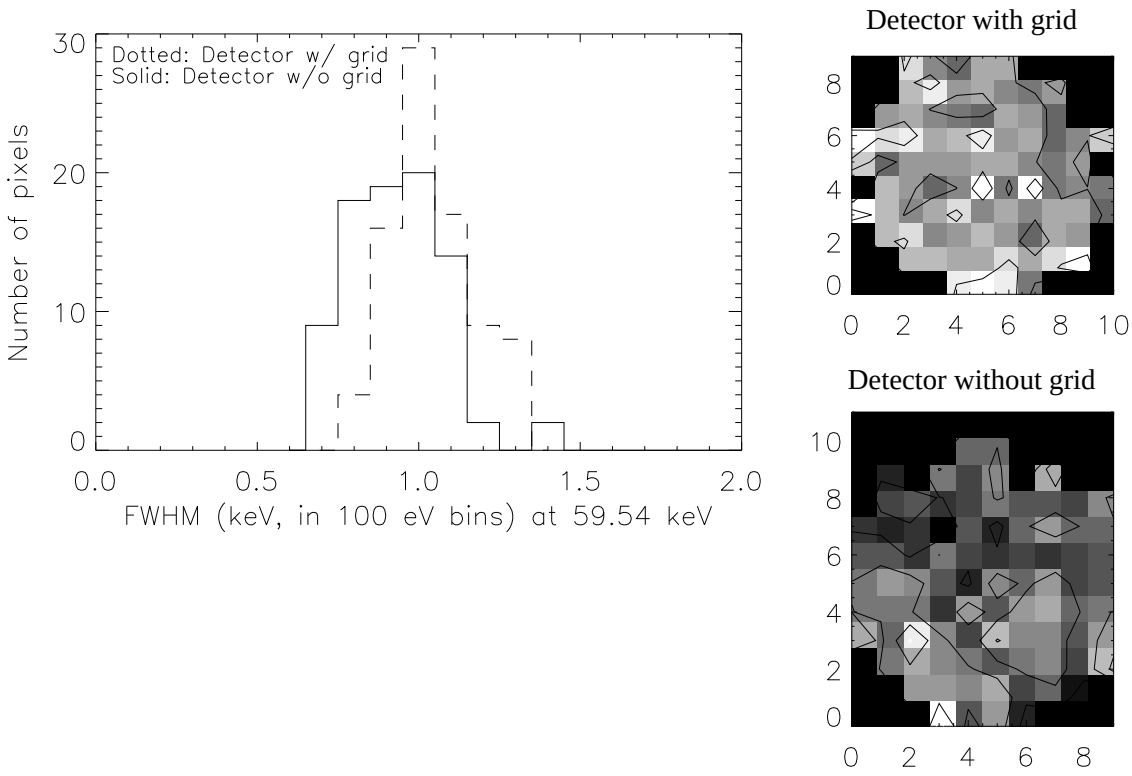

Figure 5. Distribution of line widths from the 59.54-keV line of ^{241}Am, at 0^oC, as measured at 11×10 pixels of each of the two detector designs. The histogram on the left shows a slightly better performance of the detector without a grid (solid) than the gridded detector. The intensity maps on the right show the spatial distribution of the line widths. Both maps are drawn with the same greyscale, with brightness proportional to the line width. Note that pixels at the corners are shielded from the source by the circular collimator opening. These pixels are not included in the histogram.

respectively. The solid and dash-dot lines in Fig. 4 show the FWHM distribution at the same 110 pixels at these biases.

For the detector without a grid, the leakage current results from the bulk leakage component only.

5.2. Spectral resolution for X-ray events

To characterize the response of the detectors to X-ray events, and thus the performance of the CdZnTe sensors, we tested the detectors with an Am-241 source collimated into a circular beam with a 10- to 11-pixel (5 mm) diameter.

5.2.1. Single-pixel events

Figure 5 shows the distribution of the 59.54-keV line widths for the 110 pixels under the collimator at each detector. The measurements were made at 0^oC, the targeted operating temperature for HEFT. The plot shows only events triggering one pixel. For the gridded detector with 10 μm indium bumps, the energy resolution ranges from 0.8 to 1.4 keV FWHM at 59.54 keV, with the majority of the pixels having 1.0 keV FWHM. For the non-gridded detector with 40 μm high epoxy and stud bumps, the average energy resolution is improved by an average of $\sim$ 0.1 keV.

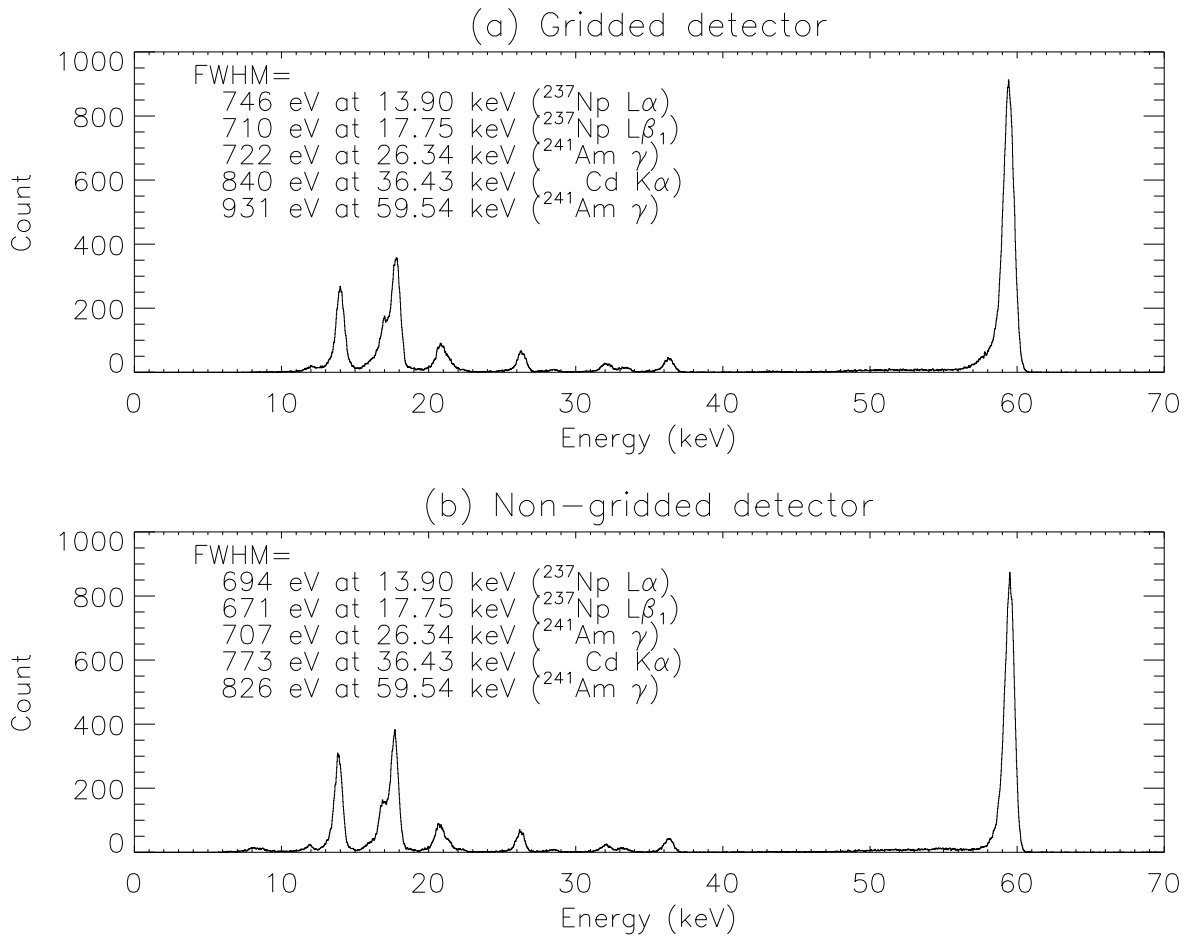

Figure 6. Spectra of ^{241}Am, from all single-pixel events summed over an 11×10 pixel area of the HEFT detectors. The Gaussian line widths as fitted from the spectra are listed. The non-gridded detector in (b) measures a more symmetric 59.54-keV line than the gridded detector in (a).

Figure 6 shows the summed spectra from all 110 pixels. Also indicated in the figure are the measured Gaussian line widths of the various spectral lines of Am-241. At low energies, the line widths are comparable to the electronic noise (the pulser line width), indicating the absence of systematic effects (e.g. incomplete charge collection) in the CdZnTe. For the gridded detector, the 59.54-keV line shows some residual low-energy tailing, with a FWHM of 931 eV. If one ignores the low-energy tail and fits the line only down to the lower half-maximum point, then the FWHM becomes 863 eV. In contrast, the non-gridded detector produces a more symmetric 59.54-keV line with a FWHM of 825 eV (756 eV if the low-energy tail is ignored).

5.2.2. Charge-sharing events

The recovery of charge-sharing events is important for detectors with pixels of this small size, since these events account for as much as 50% of the total.[4] Figure 7 shows the spectra from the two detectors obtained from charge-sharing events only. The 59.54-keV line measures a FWHM of 1.83 keV from the gridded detector, and 1.18 keV from the non-gridded detector. It has come as a surprise to us that the non-gridded detector, with its narrower interpixel gaps, does better than the gridded detector, with its steering electrodes. When single-pixel and charge-sharing events are both summed together, the spectra thus produced are shown in Figure 8. The FWHM measurements are 1.23 keV and 973 eV for the gridded and non-gridded detectors, respectively.

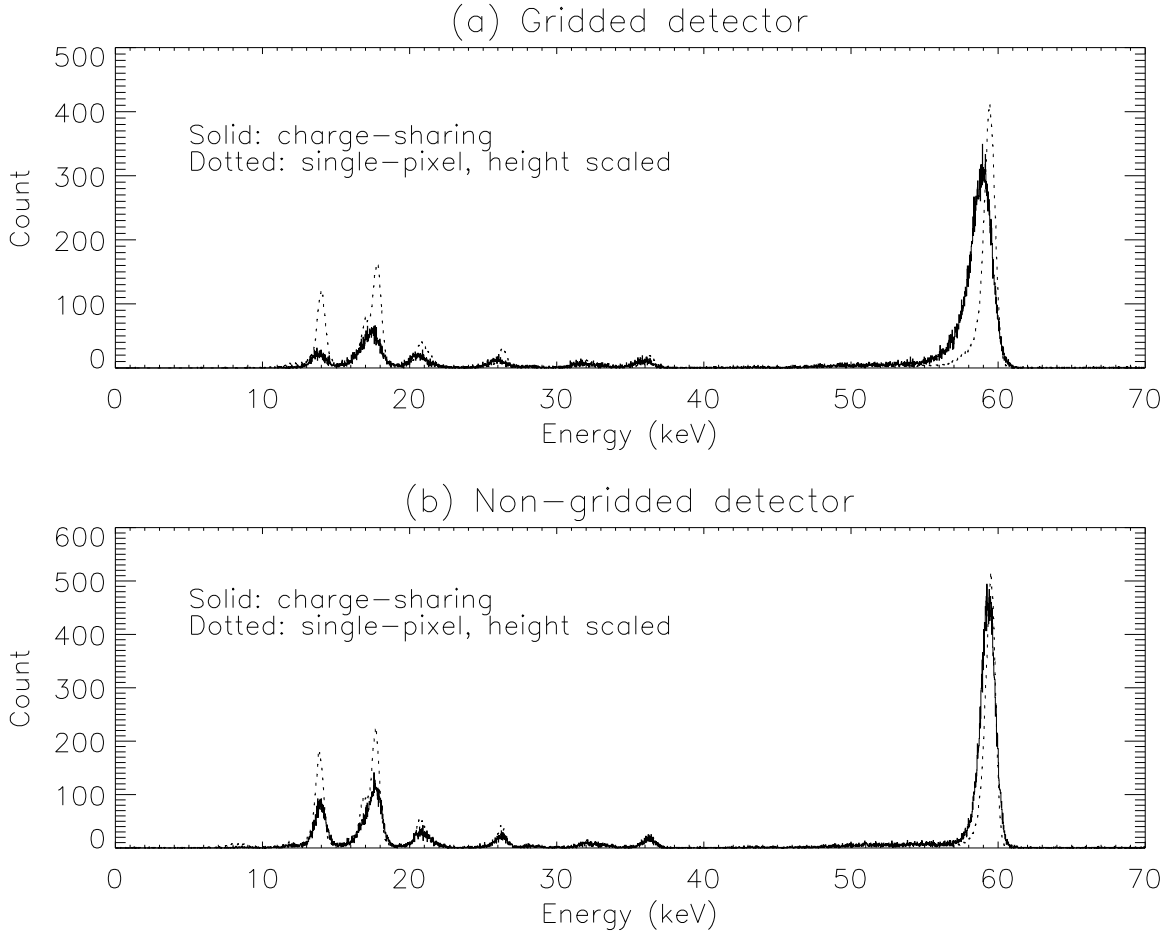

Figure 7. Spectra of ^{241}Am, from all 2-pixel charge-sharing events summed over an 11×10 pixel area of the HEFT detectors. For comparison, the spectra from single-pixel events are scaled to the same count rate and displayed here in dotted lines.

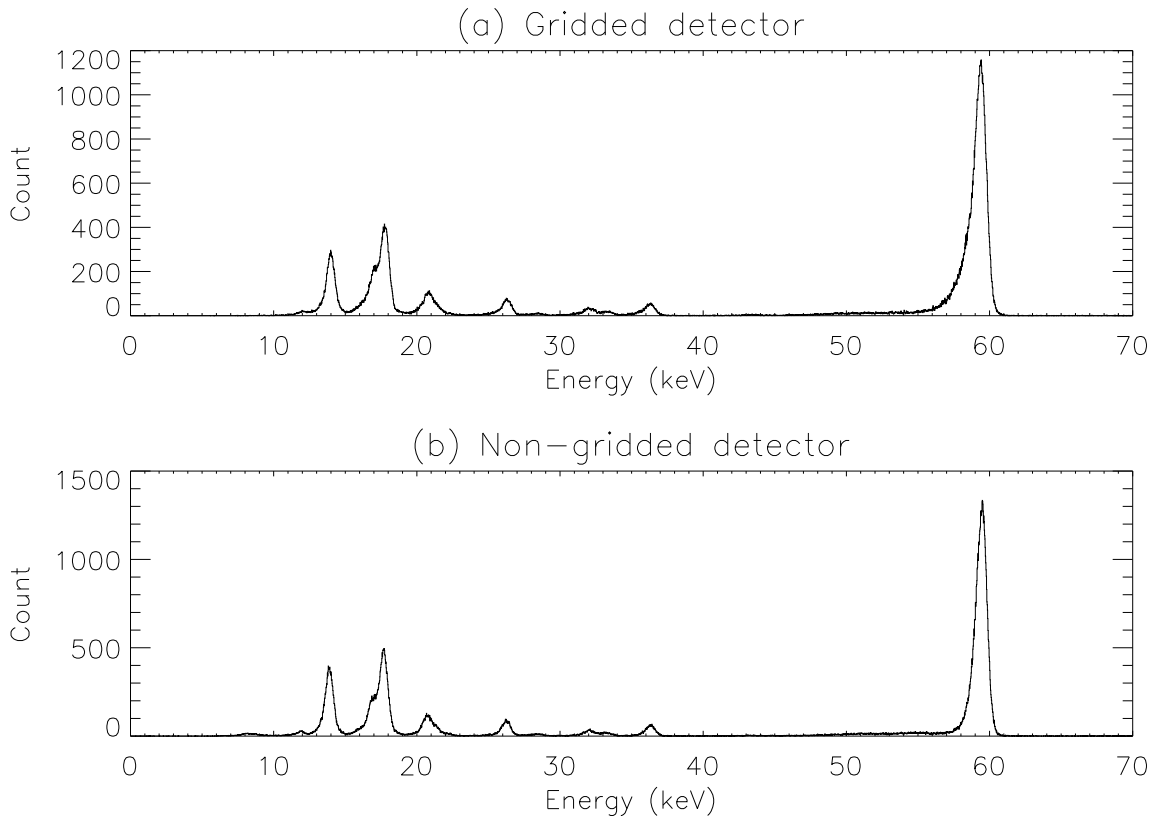

Figure 8. Spectra of ^{241}Am, from all events summed over an 11 × 10 pixel area of the HEFT detectors.

5.3. Optimization of operating biases for the gridded detector

To minimize charge trapping in the CdZnTe crystal, electrode biases have to be tuned appropriately. We measured the energy resolution of the 59.54-keV line at various bias combinations at the cathode and steering electrode of the gridded detector. For each configuration we measured the width (FWHM) and skewness of the line. Figure 9 shows their trend as a function of the bias voltages. We see that while greater grid-to-anode biases are always desirable up to −4 V (producing a surface field strength of 4 V/50μm = 80 000 V/m), cathode biases that are too large will reduce the relative grid bias ($E_{grid-anode}/E_{cathode-anode}$), and thus reduce the steering effect of the grid and increase tailing of the spectral line. On the other hand, cathode biases that are too low decrease the electron mean free path through the crystal, thus increasing charge trapping and subsequently the line width. Therefore, we need to find a balance between the two effects; according to our measurements, a −450 V cathode bias is appropriate (producing a bulk field strength of 450 V/2 mm = 225 000 V/m).

6. CONCLUSION

The HEFT detectors are optimized to achieve good energy resolution with low power. By careful design of the ASIC circuitry and off-chip digital data processing, we have achieved energy resolutions below 1 keV FWHM at hard X-ray energies, for a large-format CdZnTe-ASIC hybrid detector at 0^oC.

With characterization completed, our detector is ready to be put into production for the upcoming HEFT balloon flights. The HEFT detectors have also found application in other fields of science. For instance, the materials science group at Caltech is adopting our detector in a new generation of Mössbauer Powder Diffractometers,[5,6] with the expectation of improving the signal-to-noise ratio from about 1:1 to about 10:1 or better; this will be extremely beneficial to the development of the novel technique of Mössbauer Diffractometry, for

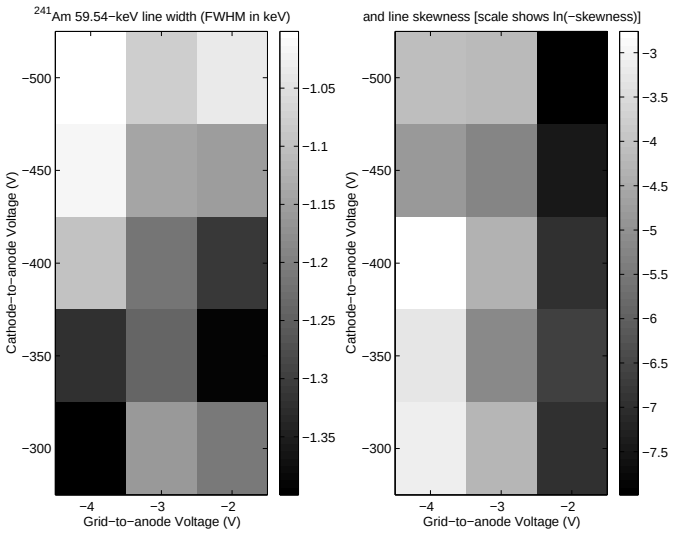

Figure 9. Intensity maps of the FWHM (left) and skewness (right) of the 59.54 keV line of ^{241}Am at various electrode bias pairs. Darkness is proportional to the FWHM magnitude on the left and to the skewness magnitude on the right, so that the most desirable configurations are the brightest ones in each case. There is a partial trade-off between FWHM and skewness.

the determination of material structures. We are also continuing to experiment with new hardware designs and software analysis approaches to improve the performance of our detector system.

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